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INSTALLATION
ORGANIZATIONAL MAINTENANCE
AND
TECHNICAL INSTRUCTIONS
FOR
SYNCHRONIZER, ELECTRICAL
SN-228(XC-2)/G

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SERVICE TEST

INSTRUCTION MANUAL

SYNCHRONIZER, ELECTRICAL, SN-228(XC-2)/G

PART I. INSTALLATION AND ORGANIZATIONAL MAINTENANCE

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SYNCHRONIZER, ELECTRICAL, SN-228(XC-2)/G

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CHAPTER 1

INTRODUCTION

Section 1. GENERAL

1. Scope of this Manual

This manual describes the installation and organizational maintenance of the Synchronizer, Electrical, SN-228(XC-2)/G. Technical instructions for the SN-228 (XC-2)/G are covered in a separate publication (Part II). Operating instructions are contained in KAO-86A/TSEC.

2. Forms and Records

a. Unsatisfactory Equipment Reports. Fill out and forward DA form A68, Unsatisfactory Equipment Report, to the Commanding Officer, U.S. Army Signal Material Support Agency, ATTN: SIGMS-MLM, Ft. Monmouth, New Jersey, as prescribed in AR 700-38.

b. Report of Damaged or Improper Shipment. Fill out and forward DD form 6, Report of Damaged or Improper Shipment, as described in AR 700-58.

c. Comments on Manual. Forward all other commments on this publication directly to the Commanding Officer, U.S.

Army Signal Material Support Agency, ATTN: SIGMS-PA2d, Ft. Monmouth, New Jersey.

Section II. DESCRIPTION AND DATA

3. Purpose and Use (fig. 1)

Synchronizer, Electrical, SN-228(XC-2)/G (herein called synchronizer) is used only with the TSEC/KW-9. The operation of TSEC/KW-9 is described in the operating manual, KAO-49A/TSEC. The synchronizer works with the teletypewriter equipment at 60 words per minute (wpm) or 100 wpm. The synchronizer maintains synchronism of TSEC/KW-9 when it is used over a marginal circuit such as long distance radio. The synchronizer permits interoperation of TSEC/KW-9 equipment at two or more stations during periods of radio fading, noise, or no transmission. It will maintain character for character synchronism during such conditions for a period of one hour. The synchronizer permits any station to send or receive and any station to stop or start the TSEC/KW-9's in synchronism.

4. Technical Characteristics

Type of signal input . . . . . . Teletypewriter 7.42 unit

	code consisting of STOP, START, and five intelligence units.
Operating Speeds:	
60 wpm (160 milliseconds per character)	Using a tuning fork frequency standard of 2000 cps.
100 wpm (98.16 milliseconds per character	Using a tuning fork frequency standard of 3260 cps.
Output to radio transmitter . .	Neutral contacts (close contact - MARK, open contact - SPACE), or 130 VDC (130 VDC - MARK, 0 VDC - SPACE), or 60 ma DC (60 ma DC - MARK, 0 ma DC - SPACE).
Input from radio receiver . . .	Neutral contacts (close contact - MARK, open contact - SPACE), or

	60 ma DC (60 ma DC - MARK 0 ma DC - SPACE).
TTY signal input	Neutral, no battery contacts from a teletypewriter KBD (keyboard) or TD (transmitter distributor).
TTY signal output	60 ma DC for a teletypewriter printer or reperforator.
General circuitry	All semiconductor digital logic circuitry consisting of 180 transistors.
Power requirements	115 volts AC ± 10%; 50 to 60 cps.
Power consumption	100 watts (approximately).

5. Table of Components

a. Components.

Quantity	Item	Height (in.)	Depth (in.)	Width (in.)	Unit weight (lb.)
1	Synchronizer, Electrical	7	16-5/8*	19	49-1/2

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a. Components (Con't).

Quantity	Item	Height (in.)	Depth (in.)	Width (in.)	Unit weight (lb.)
	SN-228(XC-2)/G (fig. 1)				
1	REC/CONV. cable			10 ft. (lg)	
1	XMTR/MOD cable			10 ft. (lg)	
1	TSEC/KW-9 cable			8 ft. (lg)	
1	T-R control cable			10 ft. (lg)	
1	Remote control box opening cover plate	4 1/4	1/8	5 1/8	
1	Remote control box bracket for mounting in AN/GRC-46 radio set	7 3/4	3/16	6	
1	Extender card for maintenance	5	3/16	13 5/8	
1	Battery shorting connector for AN/GRC-46 radio set				

* (16 inches with remote control box cable and storage brackets removed)

b. Running Spares.

Quantity	Item
1	Plug-in card A, character regenerator
1	Plug-in card B, binary divider and phase corrector
1	Plug-in card C, distributor
1	Plug-in card D, extensor
1	Plug-in card E, extractor
1	Plug-in card F, binary divider
1	Plug-in card G, output control
1	Plug-in card H, start-stop
1	Plug-in card I, delay corrector
1	Plug-in card J, main signal integrator
1	Fuse, 1 1/2 ampere
1	Fuse, 1/2 ampere
1	Lamp, 12 volt
1	Lamp, 120 volt
2	Lamp, 24 volt
1	Relay, polar

6. Description of the Synchronizer

a. The synchronizer consists of a main chassis 17 inches wide by 7 inches high by 16 inches deep fixed to a front panel 19 inches wide by 7 inches high for rack mounting. The assembled unit is shown in figure 1.

b. The synchronizer has a remote control box which houses the most frequently used operator controls. The remote control box may be located on the front panel as shown in figure 1, or it may be removed from the front panel and located at a more convenient place for the operator (figure 2).

c. All other operating controls are on the front panel of the synchronizer. All input and output connectors as well as the power cord are located on the rear panel.

7. Description of Accessory Components (fig. 3)

a. T/R Control Cable. This cable is 10 feet long and is used to connect the SN-228(XC-2)/G SEND-MARK HOLD-RECEIVE switch to the radio set SEND-RECEIVE switching circuitry.

b. REC/CONV Cable. This cable is 10 feet long and is used to connect the radio set receiver converter to the SN-228(XC-2)/G.

c. TSEC/KW-9 Cable. This cable is 8 feet long and is used to connect the TSEC/KW-9 to the SN-228(XC-2)/G.

d. XMTR/MOD Cable. This cable is 10 feet long and is used to connect the radio set transmitter modulator to the SN-228(XC-2)/G.

e. Battery Shorting Connector. This connector is used as a shorting plug in the BATTERY JACK of the AN/GRC-46 interconnecting box.

f. Remote Control Box Bracket. This bracket is used to hold the SN-228(XC-2)/G remote control box when used in the AN/GRC-46.

g. Extender Card. The extender card is installed between a logic card and its jack to raise the card for accessibility.

h. Remote Control Box Opening Cover Plate. This cover plate is installed in place of the remote control box panel when the remote control box is removed from the synchronizer.

8. Additional Equipment Required

The following additional equipment (not furnished) is required for operation.

a. TSEC/KW-9 with serial number above 1800 or with the suffix "A" after its serial number.

b. Radio transmitter and receiver with suitable input and output devices such as FSK modulator and converter. The radio equipment in the AN/GRC-46 is suitable for this purpose.

c. Teletypewriter input devices such as a keyboard (KBD) and a transmitter-distributor (TD), and teletypewriter output devices such as printer and reperforator. Teletypewriter equipment in the AN/GRC-46 is suitable for this purpose.

9. Types of Operation

The combination of the synchronizer and TSEC/KW-9 may be used in either half-duplex operation or full-duplex operation. Figure 4, is a block diagram showing the general relation between equipment in radioteletype systems.

a. Half-Duplex Operation. One synchronizer, one

TSEC/KW-9, and one half-duplex type radio set are required at each network station. In general, the greatest station separation should not exceed 500 miles. When planning to use the synchronizer in a new radio system, the best system operation will be obtained when the signal delay between transmitter modulator input and receiver output is 4 to 7 ms. An AN/GRC-46 radio set usually has a time delay within this range.

b. Full-Duplex Operation. Two synchronizers, two TSEC/KW-9's, one radio transmitter, and one radio receiver are required at each full-duplex station. In this type of operation, the signal delay is not important. The short term variation in signal delay (signal jitter) should not exceed 5 ms. Long term variation in signal delay is not important.

(PART I)

CHAPTER 2

INSTALLATION AND OPERATION

Section I. SERVICE UPON RECEIPT OF EQUIPMENT

10. Unpacking

The synchronizer is shipped in a wooden packing case with a removable top cover.

a. Remove the screws holding the top cover of the wooden packing case and remove the cover; lift the synchronizer out of its packing case.

b. Remove the cables from the compartment within the case.

11. Checking Unpacked Equipment

a. Inspect the equipment for any loss or damage that might have occurred during shipment.

b. Check the contents of the packing case against the table of components, paragraph 5c. If any of the equipment has been damaged or is incomplete, refer to paragraph 2.

12. Installation of Synchronizer in AN/GRC-46 Radio Set

Make the following installation with the power off. The synchronizer is shipped with proper internal connection options for the AN/GRC-46 radio set. A cording diagram is shown in figure 5.

a. Remote Control Box Installation.

(1) Remove the top cover of the synchronizer by a quarter turn of the five fasteners in the top cover.

(2) Remove the connector labeled REMOTE BOX on the rear of the synchronizer and unwind the remote box cable from its storage brackets.

(3) Withdraw the four captive screws on the front panel of the remote control box.

(4) Remove the remote control box from the front panel of the synchronizer and pass the cable through the opening.

(5) Install the remote box opening cover plate on the front panel of the synchronizer in place of the remote box panel. Four captive screws are supplied with the cover plate. Screw the remote control box to the remote control box bracket (fig. 3) provided with

the equipment.

(6) Remove the original cable and connector marked MARK-HOLD-SEND-RECEIVE SWITCH from the left side of the AN/GRC-46 interconnecting box.

(7) Remove the four screws holding the original SEND-REC-MARK-HOLD switch bracket to the teletype equipment slides, and remove the original cable, connector, switch, and bracket assembly from the radio set.

(8) Install the new remote control box and bracket in place of the original SEND-REC-MARK-HOLD switch bracket with the same four screws.

(9) Reconnect the remote control box cable to the rear of the synchronizer. A picture of the completed installation in shown in figure 2.

(10) Replace the top cover of the synchronizer.

b. TT-98B/FG Teletypewriter Connections.

(1) Remove the cover of the TT-98B/FG teletypewriter set.

(2) Disconnect the strap that normally connects binding posts number 2 and number 3.

(3) Remove the cord set lugs from the binding posts

and select one cord set.

(4) Connect its black wire lug to binding post number 3 and its white wire lug to binding post number 4.

(5) Tag the cord set PRINTER and insert its plug in either jack marked PRINTER on the rear of the synchronizer.

(6) Select a second cord set, and connect its black wire lug to binding post number 2 and its white wire lug to binding post number 5.

(7) Tag this cord set KBD, and insert its plug in the jack marked KBD on the rear of the synchronizer.

(8) Change the switch marked DC POWER to the OFF position.

(9) Turn the LINE CURRENT rheostat to its maximum clockwise position.

(10) Replace the cover of the TT-98B/FG.

CAUTION: The TT-98B/FG must be operated with the DC POWER switch OFF or the SN-228(XC-2)/G may be damaged.

c. TT-76A/FG Teletypewriter Connections.

(1) Locate the red and gray phone plugs of the TT-76A/FG teletypewriter reperforator.

(2) Insert the red plug into either jack marked PRINTER on the rear of the synchronizer.

(3) Insert the gray plug into the jack marked TD on the rear of the synchronizer.

(4) Install the TD control plug into the jack marked TD CONTROL on the rear of the synchronizer. If the TD control cord has not previously been installed on the TT-76A/FG, perform the modification in accordance with MWO 11-5815-224-30/1.

d. AN/GRC-46 Interconnecting Box Connections.

(1) Remove all teletypewriter plugs from the interconnecting box J-668/GR.

(2) Connect the XMTR/MOD cable to its connector on the rear of the synchronizer. The connectors are keyed to prevent improper connection.

(3) Route this cable to the rear of the teletypewriter equipment mounting structure and insert the phone plug at the opposite end of this cable into the SYNC OUTPUT jack at the right side

of the interconnecting box.

(4) The wire at the end of this cable should be connected to the binding post marked TTY LINE at the right side of the interconnecting box. No other wires should be connected to the interconnecting box binding posts.

(5) Connect the REC/CONV cable to the connector at the rear of the synchronizer and insert the phone plug at the opposite end into the jack marked SYNC OUTPUT at the left side of the AN/GRC-46 interconnecting box.

(6) Remove the cable which is inserted in the connector marked BATTERY at the left side of the interconnecting box.

(7) Install the battery shorting connector (fig. 3) in the receptacle marked BATTERY.

(8) Connect the T-R CONTROL CABLE to its connector on the rear of the synchronizer.

(9) Connect the other end of the cable to the connector marked MARK-HOLD-SEND-REC SWITCH on the left side of the interconnecting box.

e. TSEC/KW-9 Connection.

(1) Remove the shorting plug from the rear connector of the KW-9.

(2) Connect the TSEC/KW-9 cable (fig. 3) to the rear connector of the TSEC/KW-9.

(3) Connect the opposite end of this cable in the connector marked TSEC/KW-9 at the rear of the synchronizer.

CAUTION: The current adjusting potentiometer on the TSEC/KW-9 must be turned MAXIMUM counter-clockwise before the synchronizer is turned on.

f. AC Power Connections.

(1) Route the power cord of the synchronizer and the power cord of TSEC/KW-9 in back of the lower shelf and plug into the right hand 115 V AC rotary converter. The grounding pin on the synchronizer power plug should be in place.

(2) Route the power cords for the teletypewriter equipment in back of the lower shelf and plug into the left hand 115 V AC rotary converter.

CAUTION: Be sure that the grounding pins or grounding lugs of the synchronizer and teletypewriter power cords are connected to the plug box ground on the rotary converters.

g. Equipment Placement.

(1) Place TSEC/KW-9 in the space provided either on the lower shelf beneath the teletypewriter printer or in the space at the left side of the shelter.

(2) Place the synchronizer in the space provided on the right side of the lower shelf.

(3) Tighten the panel retaining nuts in the slots on the front panel of the synchronizer.

13. Installation of Synchronizer in AN/GRC-26D Radio Set

Electrical installation details only are given in this manual because physical placement of the security equipment is not known at the time of publication. A cording diagram is shown in figure 6.

a. Synchronizer Internal Connection Changes.

(1) Remove the nine screws holding the synchronizer bottom cover and remove the bottom cover.

(2) Locate the terminal board (fig. 8).

(3) Connect the red and white wire to the

XMTR INPUT-terminal.

(4) Connect the red wire to a GND terminal.

(5) Connect one of the short jumper wires to a 60 ma+ terminal and to the XMTR INPUT+ terminal.

(6) Connect the violet and white wire to the RCVR INPUT- terminal.

(7) Connect the violet wire to a GND terminal.

(8) Connect the other short jumper wire to a GND terminal and to a RCVR INPUT+ terminal.

(9) Replace the synchronizer bottom cover and nine screws.

b. TT-98B/FG Teletypewriter. The connections are made as described in paragraph 12b.

c. TT-76A/FG Teletypewriter. The connections are made as described in paragraph 12c.

d. AN/GRC-26D Radio Set Control C-1123/GRC Connections.

(1) Remove all teletypewriter plugs from Radio Set Control C-1123/GRC.

(2) Connect the T-R control cable to its connector on the rear of the synchronizer.

(3) Connect the other end of the T-R control cable

to the TTY SWITCH connector (J-2) on the control unit.

(4) Connect the XMTR/MOD cable to its connector on the rear of the synchronizer.

(5) Insert the XMTR/MOD plug into TD jack (J-9) on the control unit.

(6) Connect the wire at the end of the XMTR/MOD cable to either E-3 or E-6 binding post (ground).

(7) Connect the REC/CONV cable to its connector on the rear of the synchronizer.

(8) Insert the REC/CONV plug into one of the red REC DX jacks (J-16 through J-19) on the control unit.

(9) Set the TELETYPE switch of the control unit NORMAL DX.

e. TSEC/KW-9 Connections. TSEC/KW-9 is connected as described in paragraph 12e.

f. AC Power. Insert the power plugs of the synchronizer TSEC/KW-9, and teletypewriters in available 115 V AC 60 cycle receptacles. CAUTION: Be sure that the ground pins or grounding lugs of the synchronizer and teletypewriter power cords are connected to the receptacle ground.

14. Installation of the Synchronizer on Other Radio Sets

Specific installation instructions for other radio sets are not given in this manual. Generalized electrical requirements information is given which should enable the installer, with sufficient knowledge of the equipment, to determine connection details. The synchronizer input and output characteristics for connection to teletypewriter equipment and radio equipment is given in paragraph 4. The installer should determine which of the options can be supplied by the radio equipment and then proceed to connect the synchronizer to accept these options.

a. TTY Equipment Connection. The TTY input from KBD or TD must be neutral contacts, no battery. Internal connections in the KBD or TD should be so arranged to provide this input. A TTY repeater relay may be employed if necessary.

b. The TTY output requires a 60 ma DC teletypewriter selector magnet. The connections in the teletypewriter should be so arranged to accept this output. If the teletypewriter does not properly operate it may be necessary to reverse the polarity of the leads.

c. Radio Equipment Connections. If the radio set will not accept the plugs on the end of the synchronizer XMTR/MOD and REC/CONV cables they must be removed and replaced by suitable connectors. Radio equipment supply options may be changed at a terminal board (fig. 8) on the underside of the chassis. The synchronizer is supplied by the manufacturer with the terminal board connected for the AN/GRC-46 radio set as shown in figure 7a. Red leads go directly to the XMTR/MOD cable and are so marked. The terminal pair marked XMTR INPUT has neutral contacts. To properly connect the transmitter or modulator, a series teletype loop must be obtained consisting of TTY contacts, TTY loop battery, series limiting resistor (2,000 ohms approximately), and transmitter relay coil. The synchronizer terminal board provides these options, if they are not available in the radio transmitter. TTY loop battery is available between the ground terminal and the terminals marked +130v. In addition, battery and series limiting resistors are available between the terminals marked GROUND and +60 ma.

d. Transmitter Connections. One must complete the series loop described above either on the synchronizer terminal board or by external components. For example, figure 7a shows connections for supplying 130 V DC to the transmitter terminals (as required for AN/GRC-46). Figure 7b shows the connections for supplying 60 ma to the transmitter terminals. Figure 7c shows the connections for supplying neutral contacts to the transmitter terminals.

e. Receiver Connections. A similar loop must be obtained for the radio receiver or converter connection. Violet leads go to the REC/CONV cable and are so marked. The terminal pair marked REC INPUT has a relay coil requiring 60 ma for MARK and 0 ma for SPACE. For example, figure 7b shows the connection for 60 ma from the receiver.

f. Polarities and Grounding. Polarities must be observed for proper operation. If the synchronizer should fail to key the transmitter or the receiver should fail to key the synchronizer because of improper polarities, reverse the leads. This should be checked in both plain and cipher operation. The only ground in the synchronizer is the negative side of the 130 V loop battery. Ground connections in the radio transmitter and receiver should not conflict with this grounding system.

Section II. INITIAL ADJUSTMENT OF EQUIPMENT

15. Operating Speed Change

The synchronizer is supplied by the manufacturer with operating speed set for 60 wpm. Operation at 60 wpm requires the use of a 2000 cps tuning fork and at 100 wpm operation, the use of a 3260 cps tuning fork is required.

a. Tuning Fork Removal. The speed of operation may be changed as follows:

(1) Remove the top cover of the synchronizer by a quarter turn of the five fasteners.

(2) Remove the six screws and top cover of the tuning fork oven (fig. 8).

(3) With a screwdriver, carefully pry loose and remove the rectangular insulating material from the top of the oven.

(4) With the thumb and forefinger, reach into the oven, release the plug locking tabs, and withdraw the tuning fork plug.

(5) Grasp the tuning fork leads firmly and pull upward to withdraw the encapsulated tuning fork from the oven chamber.

b. Spare Tuning Fork. The spare tuning fork is stored in a case directly adjacent to the tuning fork oven, figure 8, and is installed as follows:

(1) Remove the two screws holding this case to the rear panel.

(2) Remove the case and withdraw the tuning fork.

(3) Lower the tuning fork into the oven chamber (2000 cps for 60 wpm, and 3260 cps for 100 wpm).

(4) With the thumb and forefinger, align the tuning fork plug with the socket in the tuning fork oven. This plug is keyed for one way insertion.

(5) After plug and socket have been aligned (some care will be required in this operation), apply enough downward pressure to engage fully the plug and locking tabs.

(6) Replace the rectangular insulating material, the tuning fork oven cover, and six screws.

(7) Insert the other tuning fork in the spare tuning fork case. Position the case and fasten it to the rear panel with the screws removed in (1) above.

c. Logic Card Changes. Certain logic cards have jumper plugs that must be repositioned as follows:

(1) Locate cards H, I, and J, shown in figure 8.

(2) Loosen the two fasteners on each rail by a quarter turn with the screw driver.

(3) Grasp the fastener on each end of the rails with each hand, exerting a steady vertical force. After the logic card is loosened, it may be withdrawn vertically upward. Care should be taken to withdraw the card slowly and straight upward to avoid damage to the card components and connectors.

(4) Figure 9, shows the jumper plugs to be changed and the position for each.

NOTE: Only the double jumper plug is to be moved on card I. The single jumper plug will disable the special character feature if it is moved.

(5) Remove the jumper plug holding screw or screws (2) from the wiring side of the card, withdraw and reposition the plugs, as shown in figure 9, and replace its holding screw or screws.

(6) One single plug on card H, one double plug on

card I, and one single and one double plug on card J, must be changed in all.

(7) Replace dards H, I, and J, in their original positions in the synchronizer chassis. The cards are keyed to prevent improper placement. Lower each card carefully into its centering rail on the base of the interconnecting board. When the connectors are engaged, press firmly downward to fully seat the card. If the card does not readily seat into position, visually check the mating of the connectors.

(8) Fix the cards in place with a quarter turn of the fasteners, and replace the top cover of the synchronizer.

d. TSEC/KW-9 Motor Speed Adjustment. Although no other modifications to the TSEC/KW-9 are required for interoperation with the synchronizer, it is important that the motor speed be set as follows:

(1) Turn on TSEC/KW-9 (it need not be connected to the synchronizer).

(2) View the white dots on the right hand motor target through the shutter of a 180 vibration-

per-second tuning fork.

(3) Best operation of both TSEC/KW-9 and the synchronizer is obtained if the TSEC/KW-9 runs about one revolution per second fast.

(4) If the motor is running slow, (the dots appear to be moving counterclockwise), grasp the worm gear adjustment shaft and gradually push in the shaft until the motion changes to a one revolution per second clockwise rotation of the dots.

(5) If after adjusting the dots are rotating clockwise faster than one revolution per second, the motor is running too fast.

(6) If the motor is running fast, pull out the worm gear adjusting shaft until the clockwise rotation of the dots slows to one revolution per second.

16. Security Interlock

a. A security interlock is provided which prevents an operator from inadvertantly sending plain text when cipher text is intended. The TD and KBD inputs are inoperative unless a plain start button is pushed. The plain start button (fig. 1) makes the TD and KBD operative only if there is no pause in input signal longer than a few seconds. In addition, there is a TD control button that energizes the TD start magnet. The plug on the TD control cable from a TT-76A/FG must be inserted into the TD CONT jack on the rear of the synchronizer.

b. If the TD control cable has not been installed on the teletypewriter, MWO 11-5815-224-30/1 must be installed on the TT-76A/FG before it is used with security equipmrnt.

c. The security interlock circuit in the synchronizer uses an internal timer with options of approximately 8 seconds, 4 seconds, and 2 seconds. The synchronizer is supplied by the manufacturer with the 4 second option connected. If the 2 or the 8 second time option is desired, make the following change:

(1) Remove the nine screws and bottom cover of the synchronizer.

(2) Locate capacitor C10 (fig. 8) and resistors R2 and R3. In the 4 second option, a violet wire is connected between one terminal of capacitor C10 and one terminal of resistor R3.

(3) If a 2 second option is desired, unsolder the blue wire from resistor R3 and resolder the wire to the blank terminal on resistor R2.

(4) If the 8 second option is desired, unsolder the blue wire and make no new connections, but insulate the end with electrical tape.

(5) Position the botton cover and fasten it in place with the nine holding screws.

17. TTY Loop Adjustments.

After installation has been completed, TTY loop currents must be adjusted as follows:

a. Turn the main power switches of the synchronizer, TSEC/KW-9, and the radio equipment to the ON position. The teletypewriter equipment need not be turned on unless they provide any of the TTY loop voltages.

b. Locate the potentiometer and meter labeled LINE ADJUST and LINE CURRENT respectively, on TSEC/KW-9.

c. Turn the potentiometer with a screwdriver until the meter reads 60 ma.

d. For AN/GRC-4 6 installation locate the meter (not labeled) and the potentiometer labeled LINE 60 MA on the juction box, and adjust the current for 60 ma.

e. On other radio sets, if the transmitter and receiver have provision for adjusting TTY loop currents, set the adjustments for 60 ma.

f. If no current is indicated or adjustments cannot be correctly made, refer to maintenance instructions.

Section III. OPERATION

18. Controls and Indicators

All operator's controls and indicators are located on the front panel or remote control box of the synchronizer. These are shown in figure 1, and described below.

Control or Indicator	Function
DELAY CORRECTOR OFF switch	Corrects for long distance radio transmission delays. Placed in OFF position for distances under 250 miles. Placed in ON position for distances over 250 miles.
CHECK-NORMAL switch	Allows "letters" check on TSEC/KW-9. Should be on CHECK position for that operation and NORMAL position at all other times.

Control or Indicator	Function
ADVANCE-RETARD switch	Advances or retards TSEC/KW-9 one letter at a time during operation. Should be momentarily pushed upward to advance one character, and momentarily pushed downward to retard one character.
STOP-START switch	Starts and stops TSEC/KW-9 in synchronism in an operating network. Position according to operating procedure.
SIGNAL-INDICATOR lamp	Indicates condition of input signal to the synchronizer. Steady mark indication is rapid flashing, steady space indication is continuously on.
SPECIAL CHARACTER switch	Initiates the special character which automatically synchronizes character phase of a network. Position according to operating procedure.
P-C switch and lamps	Switches the TTY equipment, synchronizer, and KW-9 to plain text (P) or

Control or Indicator	Function
	cipher (C). The switch is interconnected with the P-C switch on TSEC/KW-9. The red lamp is on when the system is in plain text and the green lamp is on when the system is in cipher, regardless of the position of the synchronizer P-C switch.
PLAIN START button	Releases the security interlock when sending in plain text. When momentarily depressed, the operator has a short time (8 seconds, 4 seconds, or 2 seconds, depending on option) to begin transmitting by KBD or TD. If the first character does not occur within this time period or a pause longer than this time period occurs between characters, transmission will be interrupted and the button must be depressed

Control or Indicator	Function
	again.
TD CONTROL button	Used for plain text sending with with a TD. This button must be held depressed for continuous transmission.
SEND-MARK HOLD-RECEIVE switch	Switches the radio set and synchronizer to send or receive. MARK HOLD position maintains the equipment in the receive state with steady mark applied to the synchronizer input terminals. Position according to operation procedure.
POWER ON switch	Powers the synchronizer. The tuning fork oven heater is not controlled by this switch and is energized when the power cord of the synchronizer is plugged into a 115 V AC supply.
AC fuse	This fuses the main power line. Replace with type 3AG 1.5 amp slow blow fuse.

Control or Indicator	Function
TTY fuse	This fuses all TTY loop power supplies in the synchronizer. Replace with type 3AG 0.5 amp slow blow fuse.

19. Operating Instructions

The operating instructions for this equipment are contained in KAO-86A/TSEC.

(PART I)

CHAPTER 3

MAINTENANCE INSTRUCTIONS

Section I. OPERATOR MAINTENANCE

20. Scope of Operator Maintenance

a. The following is a list of maintenance duties normally performed by the operator of the SN-228(XC-2)/G. These procedures do not require special tools or test equipment.

b. Operator maintenance consists of the following:

- (1) Preventive maintenance and visual inspection (paragraph 21).
- (2) Equipment performance checklist (paragraph 22).

21. Preventive Maintenance and Visual Inspection

The following preventive maintenance should be performed weekly.

a. Check completeness and general condition of equipment.

b. Clean dirt and moisture from switches, jacks, plugs, and panels.

c. Inspect controls for normal operation.

d. Check for normal operation of equipment. Be alert for unusual operation or conditions.

e. Clean and tighten exteriors of cases and mountings.

f. Inspect cases, mounts, and exposed metal surfaces for corrosion.

g. Inspect cords, cable, and wire for cuts, kinks, breaks, fraying, and undue strain.

h. Inspect accessible items for looseness. Logic cards, switches, connectors, relays, and pilot lights.

22. Equipment Performance Check List

a. General. This check list is used to check systematically, equipment performance and help the operator sectionalize the trouble. All corrective measures which the operator can perform are given in the corrective measures column. If the action taken by the operator does not correct the fault, additional maintenance must be performed by maintenance personnel having adequate tools, test equipment, and authority. The operator should note on the repair tag how the equipment performed and what corrective measures were taken. In using the check list start at the beginning and follow each step in order to locate the trouble. However, if trouble is suspected in any particular area, start checking at that point and continue the steps sequentially.

b. Check List.

Action or Condition	Normal Indication	Corrective Measures
Power switch in ON position.	AC indicator lamp is on.	Check for AC power at plug. Check and replace AC fuse, check and replace AC pilot lamp.
TSEC/KW-9 and synchronizer P-C switch in P position.	P (red) lamp lights.	Replace P (red) lamp.
TSEC/KW-9 and synchronizer P-C switch in C position.	C (green) lamp lights.	Replace C (green) lamp.
With P-C switch in P position, SEND-MARK HOLD RECEIVE switch in SEND position and PLAIN START	Teletypewriters should print home copy and the radio transmitter should send teletype characters	Check and replace TTY fuse on front panel of synchronizer, check cabling for conformance to cording chart, check

b. Check List. (Con't)

Action or Condition	Normal Indication	Corrective Measures
button momentarily depressed send KBD or TD message.		tightness of all connectors. Make required operator checks of TTY and radio equipment described in the individual equipment manuals.
With P-C switch in P position and SEND-MARK HOLD-RECEIVE switch in RECEIVE position tune the radio receiver to any plain text teletype signal of the proper speed.	Teletypewriters should print text.	Check cabling for conformance to cording chart. Check connectors for tightness. Make operator check of TTY and radio equipment as described in those manuals.
TSEC/KW-9 and synchro-	Signal indicator lamp	Replace signal indicator

b. Check List. (Con't)

Action or Condition	Normal Indication	Corrective Measures
nizer P-C switches in C position. SEND-MARK HOLD-RECEIVE switch in SEND position	should rapidly flash on and off.	lamp if completely off.

Section II. ORGANIZATIONAL MAINTENANCE

23. Scope of Organizational Maintenance

Organizational maintenance of the SN-228(XC-2)/G consists of the following:

a. Preventive maintenance and visual inspection (par. 25).

b. Trouble-shooting check list (par. 26).

c. Replacement of plug-in logic cards (par. 27).

d. Replacement of plug-in relays (par. 27).

e. Replacement of defective connectors and cables (par. 26).

f. Loop current adjustments (par. 17).

24. Tools and Test Equipment Required

The tools and test equipment required for organizational maintenance are listed below.

a. Tool equipment TE-50B.

b. Multimeter AN/URM-105.

25. Preventive Maintenance and Visual Inspection are the same as for the operator (par. 21).

26. Trouble-Shooting Check List

The chart below is furnished to help sectionalize trouble in the synchronizer to a particular section or logic card. Only those corrective measures which the organizational maintenance man can accomplish are given. If the measure suggested does not restore normal equipment performance, trouble-shooting is required at a field maintenance level. Note on the repair tag what corrective measures were taken.

a. Before using the trouble-shooting check list, examine the repair tags to determine whether the trouble has been sectionalized. If there has been no sectionalization, perform the procedures outlined in the equipment performance check list given in paragraph 22.

b. Trouble-Shooting Check List.

WARNING: Turn the synchronizer power switch OFF before removing or replacing a card.

b. Trouble-Shooting Check List.

Symptom	Probable Trouble	Correction
Power switch ON, TSEC/KW-9 and synchronizer P-C switch in C position, SEND-MARK-HOLD-RECEIVE switch in SEND position, SIGNAL INDICATOR lamp off.	Defective power supply.	Check power supply voltages as follows: locate feed through capacitors C23, C24, and C25 in bulkhead separating power supply compartment. With respect to ground check C23 for -24V DC. Check C24 for -12 V DC. Check C25 for +6 V DC. If any voltage is more than 20% higher from required value refer to higher echelon maintenance.
Same	Defective card J.	Replace card J. If replacement does not clear trouble, refer to higher echelon for maintenance.

b. Trouble-Shooting Check List (Con't)

Symptom	Probable Trouble	Correction
Indicator lamp is on but not flashing.	Logic circuits are not reset, synchronizer input not on steady mark.	Turn power switch off for several seconds then turn on. Remove TTY plugs from jacks marked KBD and TD in rear of synchronizer. If lamp begins flashing trouble is in signal circuits of KBD or TD.
Same	Tuning fork inoperative.	Open tuning fork oven, check tightness of tuning fork connector If new tuning fork is available, make a replacement.
Same	Defective cards J, B, or A.	Replace cards J, B, and A in that order one at a time. If a particular card remedies the trouble, use only that card as a replacement.

b. Trouble-Shooting Check List (Con't)

Symptom	Probable Trouble	Correction
		If this does not clear trouble, refer to higher echelon for maintenance.
TSEC/KW-9 does not begin operating approximately 8 seconds after STOP-START switch is changed to START position.	Faulty cable between synchronizer and TSEC/KW-9.	Check connectors on rear of TSEC/KW-9 and synchronizer or replace entire cable.
Same	Defective card H.	Replace card H.
Same	Defective relay K1.	Locate and replace relay K1 on bottom side of synchronizer chassis. If this does not clear the trouble, refer to higher echelon

b. Trouble-Shooting Check List (Con't)

Symptom	Probable Trouble	Correction
		for maintenance.
Lack of, or improper home copy during TTY signal transmission.	Synchronizer logic circuitry improperly reset.	Turn synchronizer power switch off for several seconds. Change SEND-MARK HOLD-RECEIVE switch to RECEIVE and then to SEND position.
Same	Defective card F, C, or D.	Replace cards F, C, and D one at a time and in that order. If trouble is not cleared refer to higher echelon for maintenance.
Change START-STOP switch to START position. Synchronizer signal does not key transmitter, or trans-	Defective card G.	Replace card G. If this does not clear trouble, refer to higher echelon for maintenance.

b. Trouble-Shooting Check List (Con't)

Symptom	Probable Trouble	Correction
mitter is continually keyed with no KBD or TD input.		
Special character does not operate transmitter or transmitter does not go to steady space for approxiamtely 8 seconds during cipher start procedure.	Defective card H.	Replace card H.
Same	Defective K2 relay.	Locate K2 relay on bottom side of synchronizer and replace it. If the trouble is not cleared, refer to higher echelon for maintenance.

b. Trouble-Shooting Check List (Con't)

Symptom	Probable Trouble	Correction
Transmitter remains on steady space and/or printer runs as if on an open line.	Defective loop voltage supply or fuse.	Check and replace TTY fuse on front panel of synchronizer. With a voltmeter, check for presence of about 140 V on rear terminal TTY fuse holder. If voltage is off by more than 30% refer to higher echelon for maintenance.
Synchronizer does not switch from SEND to RECEIVE when SEND-MARK HOLD-RECEIVE switch is changed (no audible clicking sound about 1/4 second after	Defective card G.	Replace card G. If trouble is not cleared, refer to higher echelon for maintenance.

b. Trouble-Shooting Check List (Con't)

Symptom	Probable Trouble	Correction
switch is changed.		
Change SEND-MARK HOLD-RECEIVE switch to MARK HOLD position. Indicator does not flash on and off rapidly.	Defective K3 relay.	Locate K3 on bottom side of synchronizer chassis and replace it. If trouble is not cleared refer to higher echelon for maintenance.
Change SEND-MARK HOLD-RECEIVE switch to the RECEIVE position. TSEC/KW-9 does not begin operating when start procedure is followed during good radio path operations.	Defective card J or H	Replace card J and H one at a time and in that order. If trouble is not cleared, refer to higher echelon for maintenance.

b. Trouble-Shooting Check List (Con't)

Symptom	Probable Trouble	Correction
Receiving printer does not operate during signal transmission or prints garble continually during no signal transmission.	Defective card G.	Replace card G. If trouble is not cleared, refer to higher echelon for maintenance.
Receiving printer prints only occasional garbled characters during continuous TD transmission.	Improper receiver phasing. Defective card E.	Replace card E. If trouble not cleared, refer to higher echelon for maintenance.
Receiving printer prints continuous garble during contin-	Improper start signal	Repeat cipher start procedure several times.

b. Trouble-Shooting Check List (Con't)

Symptom	Probable Trouble	Correction
uous TD transmission.		
Same	Improper phasing in receiving synchronizer. Defective card I	Replace card I and repeat cipher start procedure.
Same	Improper phasing from transmitter synchronizer.	Request organizational maintenance man at transmitting station to replace I. Resynchronize network and initiate start procedure.
Same	Improper TSEC/KW-9 adjustment or defective TSEC/KW-9.	Perform TSEC/KW-9 Maintenance as described in its maintenance manual. If this does not clear trouble refer to higher echelon for maintenance.

27. Removal and Replacement of Parts

a. Removal and Replacement of Logic Cards. The logic cards are identified by a letter A through J marked on the upper sides of their supporting rails (fig. 8). Remove cards as follows:

(1) Remove the top cover by releasing the five quarter-turn fasteners.

(2) Release the two fasteners on each rail by a quarter turn with a screwdriver.

(3) Grasp the fasteners on each end of the rail with each hand and exert a steady force upwards. After the logic card is loosened, it may be withdrawn vertically upward. Care should be taken to withdraw the card slowly and straight up to avoid damage to the card components and connectors.

(4) To return the card to its station, lower card carefully into its centering rail on the base of the interconnecting board. When the connectors are engaged, press firmly downward to fully seat the card into position, check the mating of the connectors.

(5) Fix the cards in place with a quarter turn of

the fasteners.

(6) Replace the top cover.

b. Removal and Replacement of Plug-In TTY Relays. Relays K1, K2, and K3 are located on the underside of the synchronizer chassis on a hinged plate (fig. 8).

(1) Remove the bottom cover, and remove the remaining four screws which hold the hinged bottom plate in position.

(2) Raise the hinged plate upward.

(3) Withdraw two screws holding the cover which retains relays K1, K2, and K3 in their sockets.

(4) Remove the relay in question.

(5) Install a new relay and replace the holding cover and two screws.

(6) Lower the hinged plate into position and replace the four holding screws.

(7) Replace the bottom cover with nine screws.

(PART I)

CHAPTER 4

SHIPMENT AND LIMITED STORAGE AND DEMOLITION TO PREVENT ENEMY USE

Section I. SHIPMENT AND LIMITED STORAGE

28. Disassembly of Equipment

Disconnect the cables from the rear of the synchronizer and remove the synchronizer from its mounting.

29. Repacking for Shipment or Limited Storage

a. The exact procedure for repacking depends on the material available and conditions under which the synchronizer is to be shipped or stored.

b. Package the synchronizer and accessory components as outlined below:

(1) Wrap the synchronizer in neutral paper. Cut a piece of plywood larger than the front panel and tape in place to protect the controls. Wrap the corrugated cardboard around the unit and tape.

(2) Wind each cable assembly into a coil of convenient dimension and tie it with cotton twine.

c. Pack the synchronizer and accessory components in a cardboard carton or wooden box. Pack filler material between and around the items as required for cushioning.

Section II. DEMOLITION OF MATERIAL TO PREVENT ENEMY USE

30. Authority for Demolition

Demolition of the equipment will be accomplished only upon the order of the commander. The destruction procedures outlined in paragraph 31, will be used to prevent further use of the equipment.

31. Methods of Destruction

Use any of the following methods to destroy the equipment:

a. Smash. Smash the controls, logic cards, switches, capacitors, transformers, and relays; use sledges, axes, handaxes, pickaxes, hammers, or crowbars.

b. Cut. Cut the cables with axes, handaxes, or machetes.

c. Burn. Burn cables and technical manuals; use gasoline, kerosene, oil, flame throwers, or incendiary grenades.

d. Bend. Bend panel and chassis.

e. Explode. If explosives are necessary, use firearms, grenades, or TNT.

f. Dispose. Bury or scatter the destoryed parts in slit trenches, foxholes, or throw them into streams.

(PART I)

APPENDIX

REFERENCES

The following is a list of applicable references available to the operator and installer of Synchronizer, Electrical, SN-228(XC-2)/G.

TM 11-264B	Radio Set AN/GRC-26D.
TM 11-2225	Teletypewriter Sets AN/GGC-3 and AN/GGC-3A, and Teletypewriter Reperforator-Transmitters TT-76/GGC, TT-76A/GGC, and TT-76B/GGC.
TM 11-5815-200-10	Operator's Manual, Teletypewriter Sets AN/FGC-20, AN/FGC-20X, AN/FGC-21, AN/FGC-64, AN/FGC-66, and AN/UGC-4, and Teleprinter TT-259/FG.
TM 11-5815-200-35	Field and Depot Maintenance Teletypewriter Sets AN/FGC-20, AN/FGC-20X, AN/FGC-21, AN/UGC-4, and Teleprinter TT-259/FG.
TM 11-5815-204-10	Operator's Manual, Radio Teletypewriter Sets AN/GRC-46 and AN/VRC-29.
TM 11-5815-204-20	Organizational Maintenance, Second Echelon, Radio Teletypewriter Sets AN/GRC-46 and AN/VRC-29.
KAO-49A/TSEC	Operation of TSEC/KW-9.
KAO-86A/TSEC	Operating Instructions for

(PART I)

Synchronizer, Electrical,
SN-228(XC-2)/G.

TB SIG 340 . . . . Cipher Machine TSEC/KW-9.

Instruction Manual for Synchronizer, Electrical, SN-228(XC-2)/G, Part II, Technical Instructions.

(PART I)

GLOSSARY

Section I. ABBREVIATIONS

cps	cycles per second
wpm	words per minute
TTY	teletype
ac	alternating current
ma	milliamperes
TD	transmitter-distributor
KBD	keyboard
dc	direct current

Section II. DEFINITIONS

Half-duplex operation. A type of radio-teletype operation that permits transmission and reception in both directions but not at the same time.

Loop. A closed extension circuit generally containing one or more teletypewriter components.

Neutral keying. Square-wave dc pulses which have a single polarity with respect to ground.

Mark. Corresponds to the closed key condition of a teletypewriter circuit.

Space. Corresponds to the open key condition of a teletypewriter circuit.

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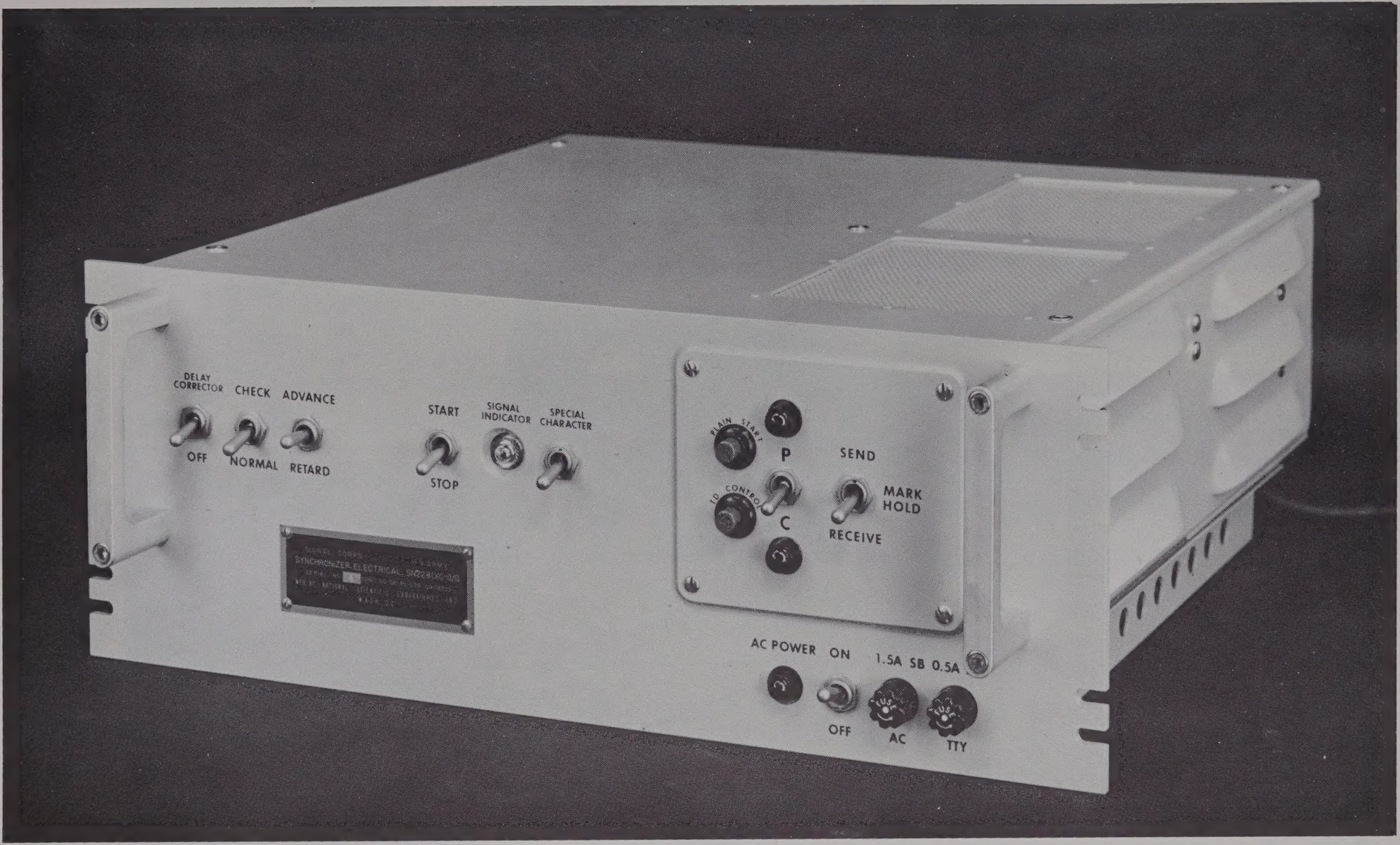

DELAY CORRECTOR
OFF
CHECK
NORMAL
ADVANCE
RETARD
START
STOP
SIGNAL INDICATOR
SPECIAL CHARACTER
PLAIN START
P
TD CONTROL
C
SEND
MARK HOLD
RECEIVE
AC POWER
ON
OFF
1.5A SB 0.5A
AC
TTY

FIG. 1. SYNCHRONIZER, ELECTRICAL, SN-228(XC-2)/G.

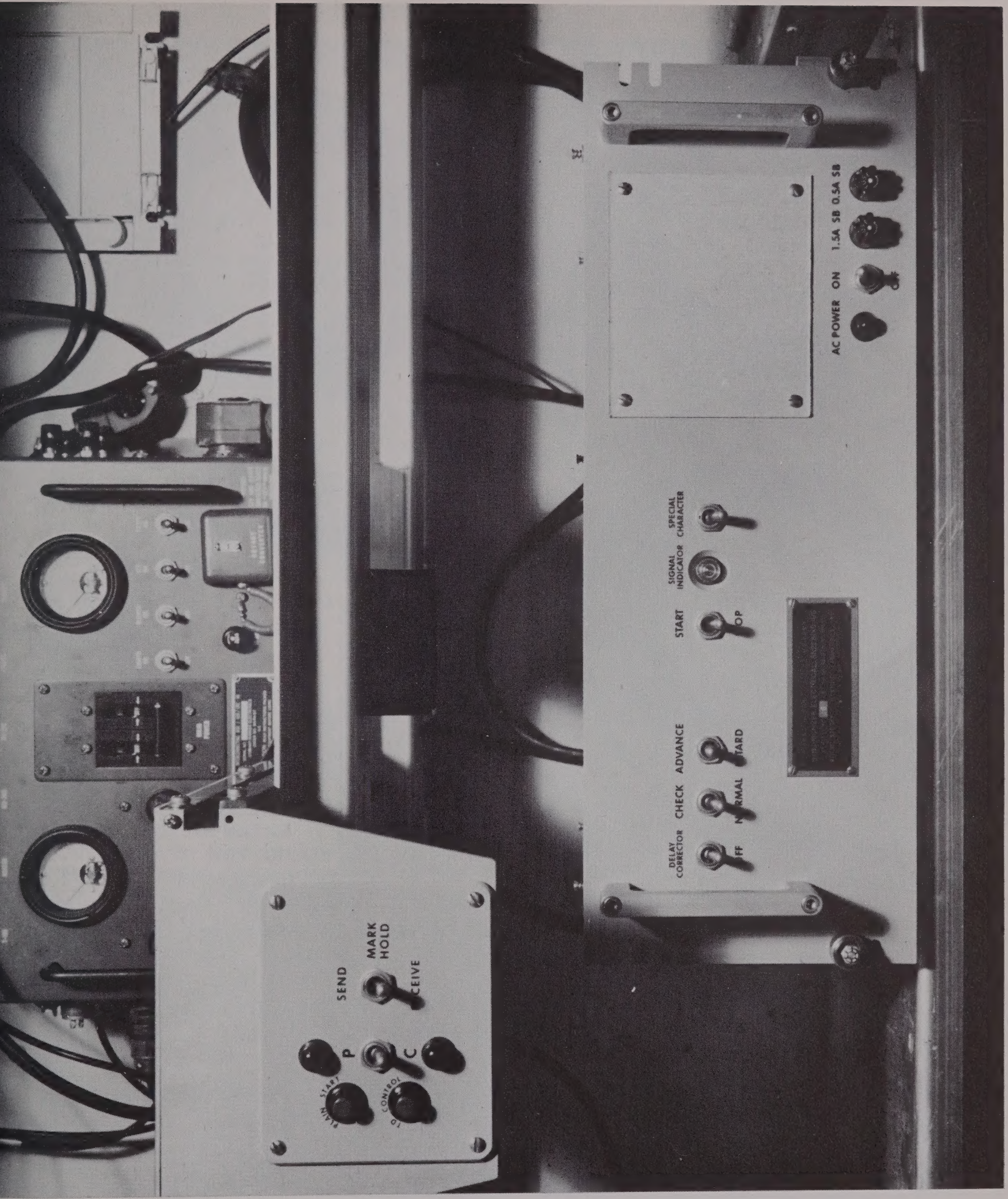

AC POWER
ON
1.5A SB
0.5A SB
SPECIAL CHARACTER
SIGNAL INDICATOR
START
DELAY CORRECTOR
CHECK
ADVANCE
SEND
MARK HOLD
P
C
START
TD CONTROL

FIG. 2. SN-228(XC-2)/G INSTALLATION IN AN/GRC-46 RADIO SET (TSEC/KW-9 AND TTY EQUIPMENT NOT SHOWN).

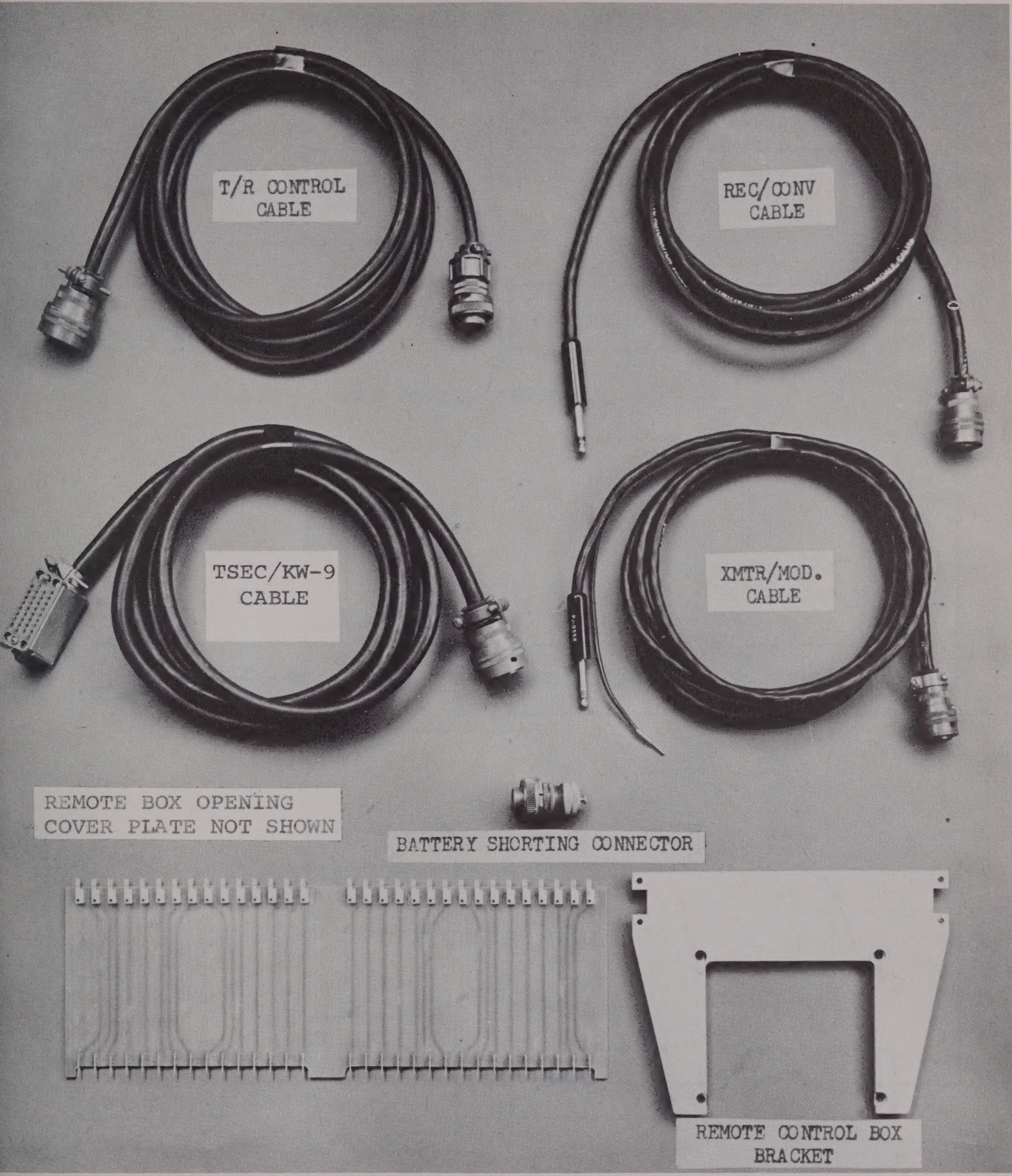
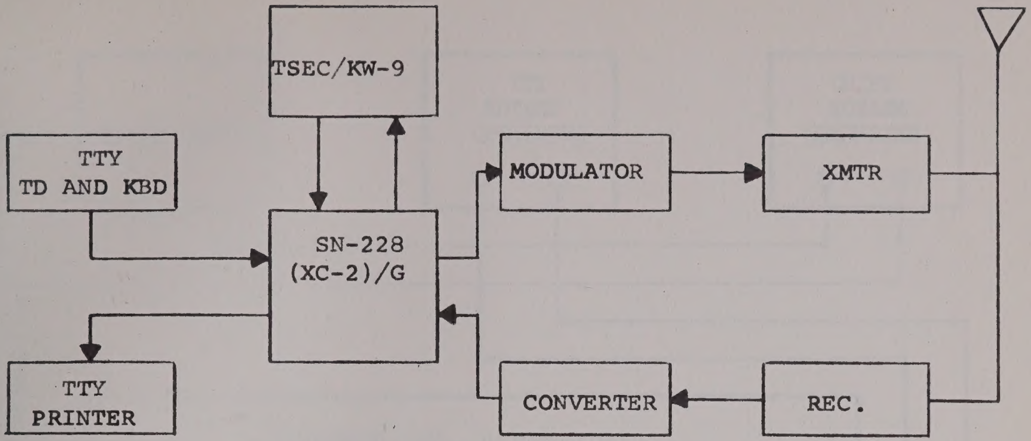
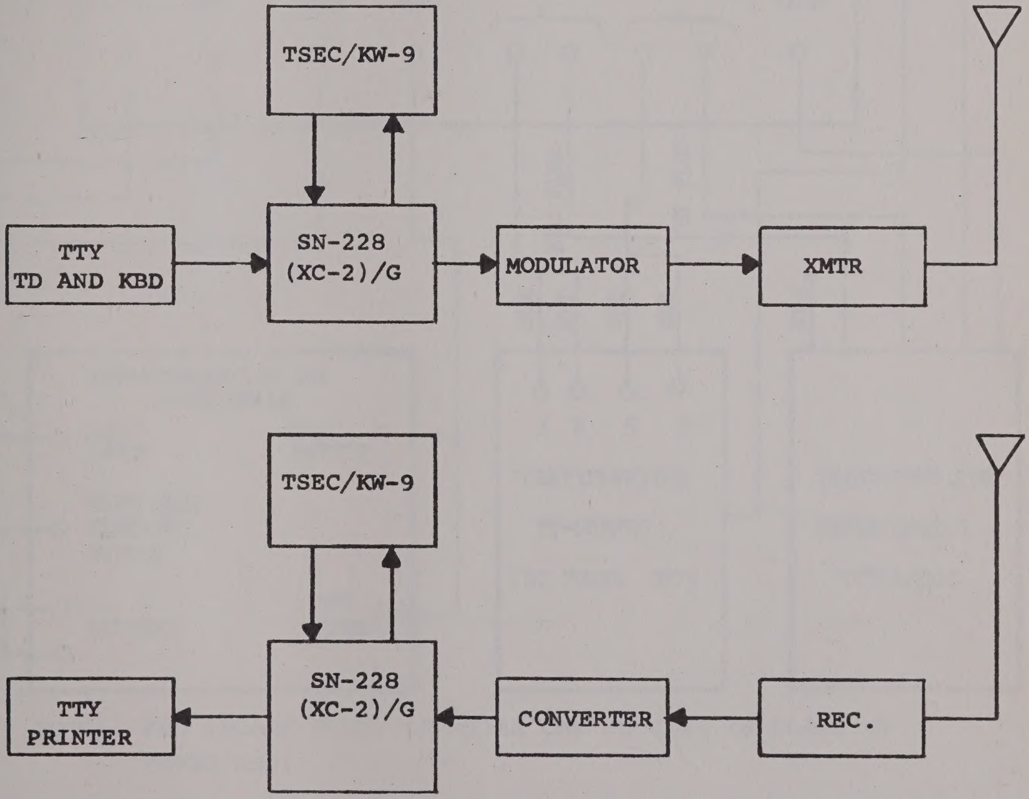

T/R CONTROL CABLE
REC/CONV CABLE
TSEC/KW-9 CABLE
XMTR/MOD. CABLE
REMOTE BOX OPENING COVER PLATE NOT SHOWN
BATTERY SHORTING CONNECTOR
REMOTE CONTROL BOX BRACKET

FIG. 3. ACCESSORY COMPONENTS FOR SN-228(XC-2)/G.

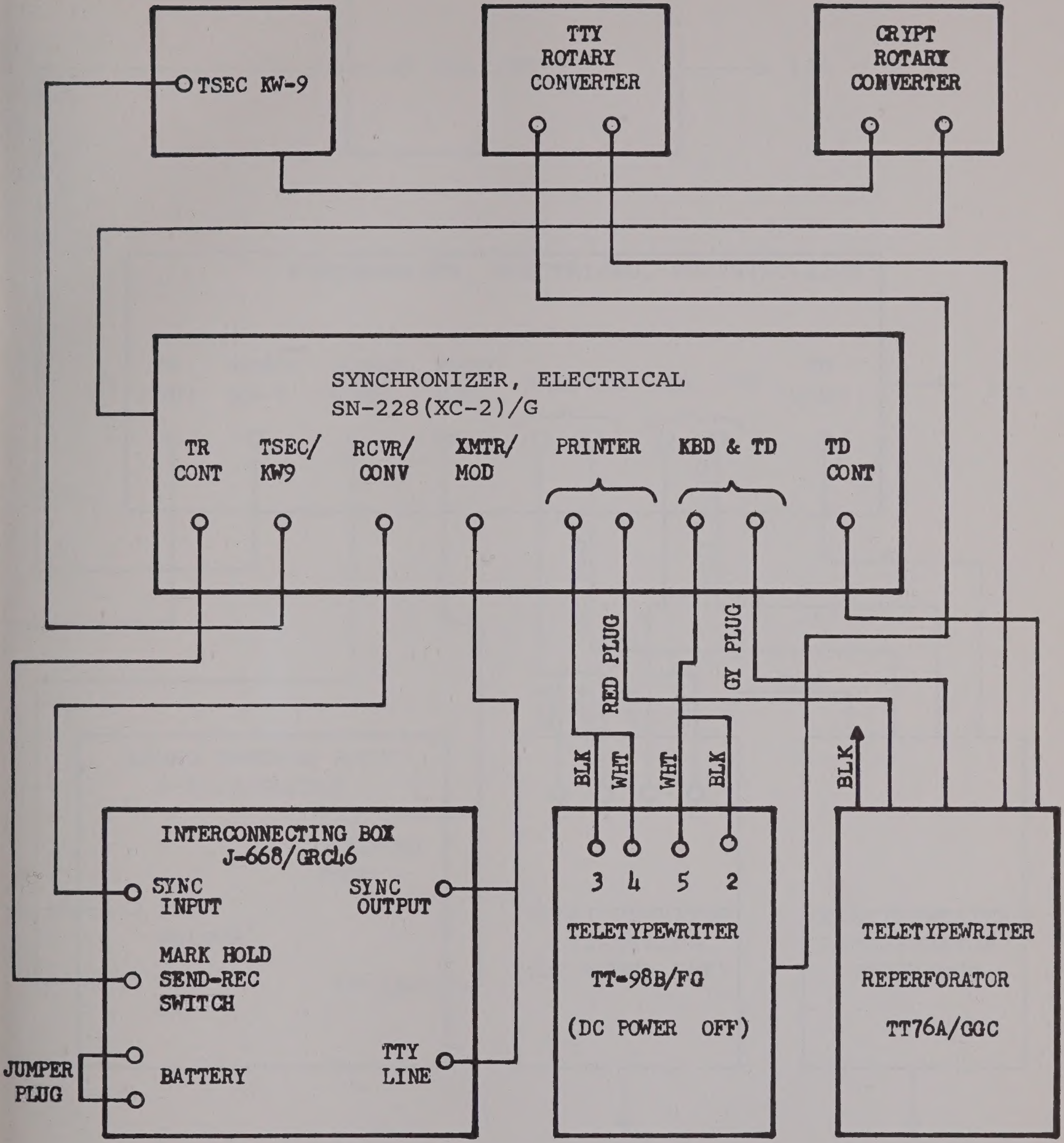

TSEC/KW-9
TTY TD AND KBD
SN-228 (XC-2)/G
MODULATOR
XMTR
TTY PRINTER
CONVERTER
REC.

A. HALF DUPLEX STATION.


TSEC/KW-9
TTY TD AND KBD
SN-228 (XC-2)/G
MODULATOR
XMTR
TSEC/KW-9
TTY PRINTER
SN-228 (XC-2)/G
CONVERTER
REC.

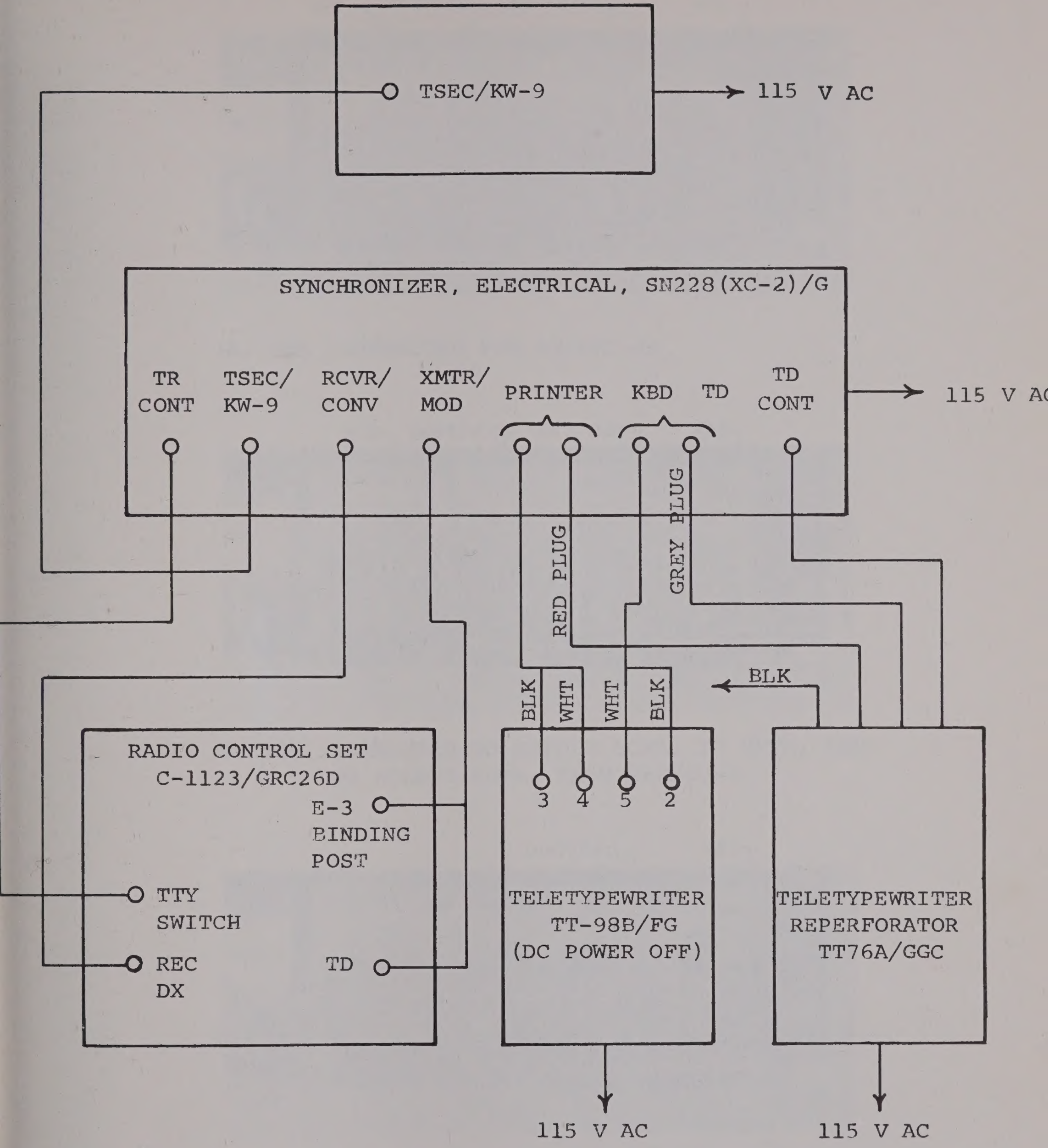
B. FULL DUPLEX STATION

FIG. 4. BLOCK DIAGRAM OF SN-228(XC-2)/G RADIOTELETYPE SYSTEMS.


TSEC KW-9
TTY ROTARY CONVERTER
CRYPT ROTARY CONVERTER
SYNCHRONIZER, ELECTRICAL SN-228(XC-2)/G
TR CONT
TSEC/ KW9
RCVR/ CONV
XMTR/ MOD
PRINTER
KBD & TD
TD CONT
RED PLUG
GY PLUG
BLK
WHT
WHT
BLK
BLK
INTERCONNECTING BOX J-668/GRC46
SYNC INPUT
SYNC OUTPUT
MARK HOLD SEND-REC SWITCH
JUMPER PLUG
BATTERY
TTY LINE
3
4
5
2
TELETYPEWRITER TT-98B/FG (DC POWER OFF)
TELETYPEWRITER REPERFORATOR TT76A/GGC

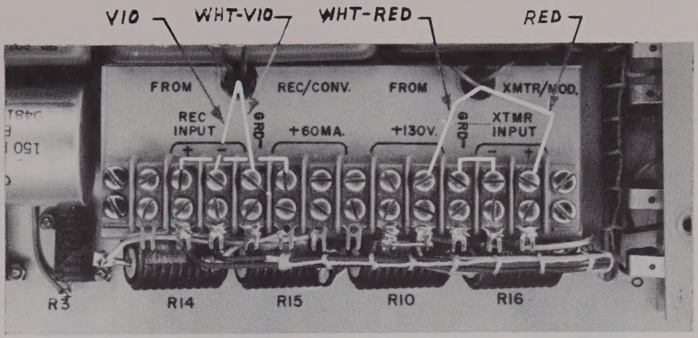
NOTE: KBD (BLACK PLUG) OF TT76A CAN BE USED IN PLACE OF TT98B KBD.

FIG. 5. CORDING DIAGRAM FOR CONNECTING SN-228(XC-2)/G to AN/GRC-46.

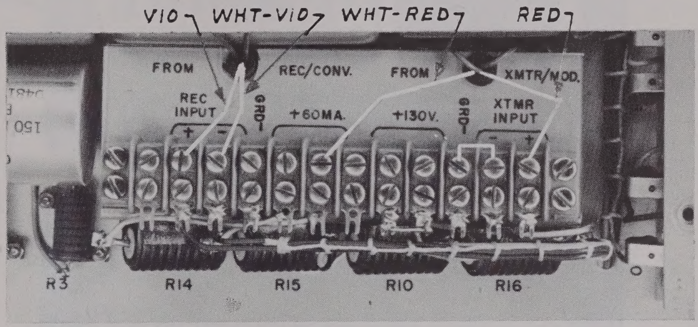

TSEC/KW-9
115 V AC
SYNCHRONIZER, ELECTRICAL, SN228(XC-2)/G
TR CONT
TSEC/ KW-9
RCVR/ CONV
XMTR/ MOD
PRINTER
KBD
TD
TD CONT
115 V A
RED PLUG
GREY PLUG
BLK
WHT
WHT
BLK
BLK
RADIO CONTROL SET C-1123/GRC26D
E-3 BINDING POST
TTY SWITCH
REC DX
TD
3
4
5
2
TELETYPEWRITER TT-98B/FG (DC POWER OFF)
TELETYPEWRITER REPERFORATOR TT76A/GGC
115 V AC
115 V AC

NOTE: KBD (BLACK PLUG) OF TT76A CAN BE USED IN PLACE OF TT98B KBD.

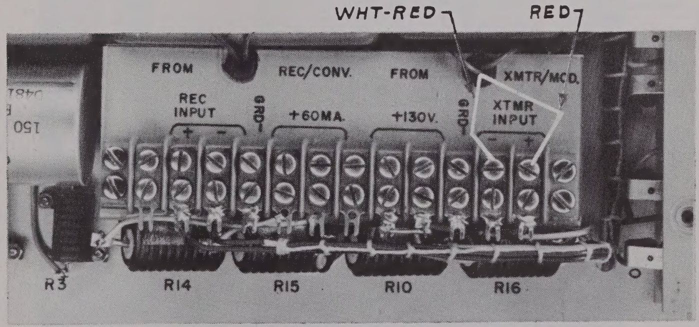
FIG. 6. CORDING DIAGRAM FOR CONNECTING SN-228(XC-2)/G TO AN/GRC-26D.


VIO
WHT-VIO
WHT-RED
RED
FROM
REC/CONV.
FROM
XMTR/MOD.
REC INPUT
+ −
GRD
+60MA.
+130V.
GRD
XTMR INPUT
− +
R3
R14
R15
R10
R16

A. TB5 CONNECTED FOR AN/GRC-46.

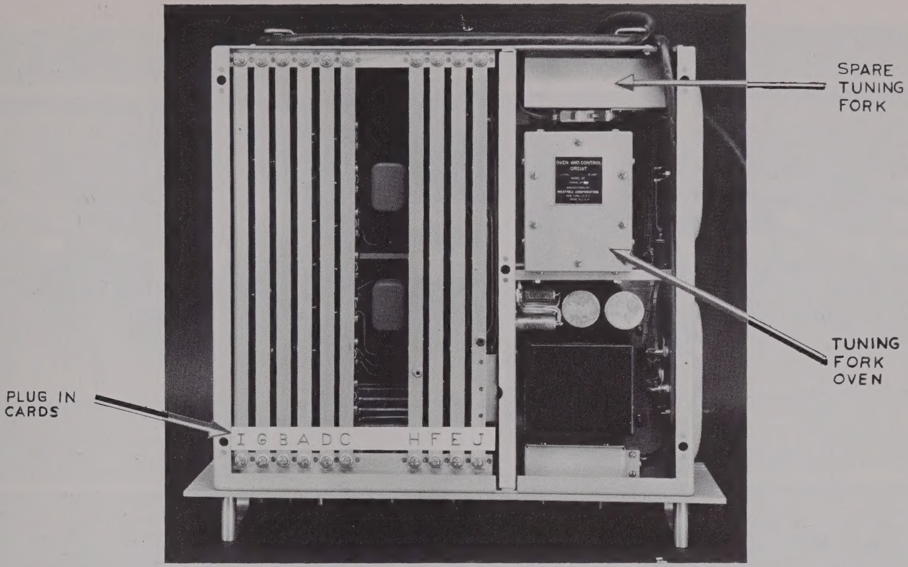

VIO
WHT-VIO
WHT-RED
RED
FROM
REC/CONV.
FROM
XMTR/MOD.
REC INPUT
+ −
GRD
+60MA.
+130V.
GRD
XTMR INPUT
− +
R3
R14
R15
R10
R16

B. TB5 CONNECTED TO SUPPLY 60MA. TO XMTR, AND TO ACCEPT 60MA. FROM REC/CONV.

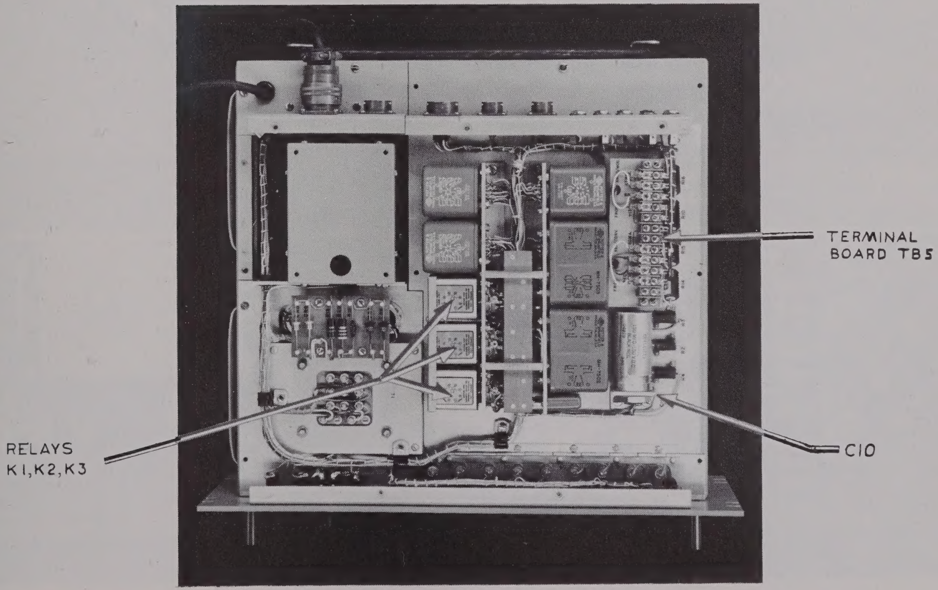

WHT-RED
RED
FROM
REC/CONV.
FROM
XMTR/MOD.
REC INPUT
+ −
GRD
+60MA.
+130V.
GRD
XTMR INPUT
− +
R3
R14
R15
R10
R16

C. TB5 CONNECTED TO SUPPLY NEUTRAL CONTACTS TO XMTR/MOD.

FIG. 7. TERMINAL BOARD OPTIONS IN SN-228(XC-2)/G.


SPARE TUNING FORK
TUNING FORK OVEN
PLUG IN CARDS
I G B A D C
H F E J

A. TOP VIEW (COVER REMOVED)


TERMINAL BOARD TB5
RELAYS K1,K2,K3
C10

B. BOTTOM VIEW (COVER REMOVED)

FIG.8. COMPONENT LOCATION.

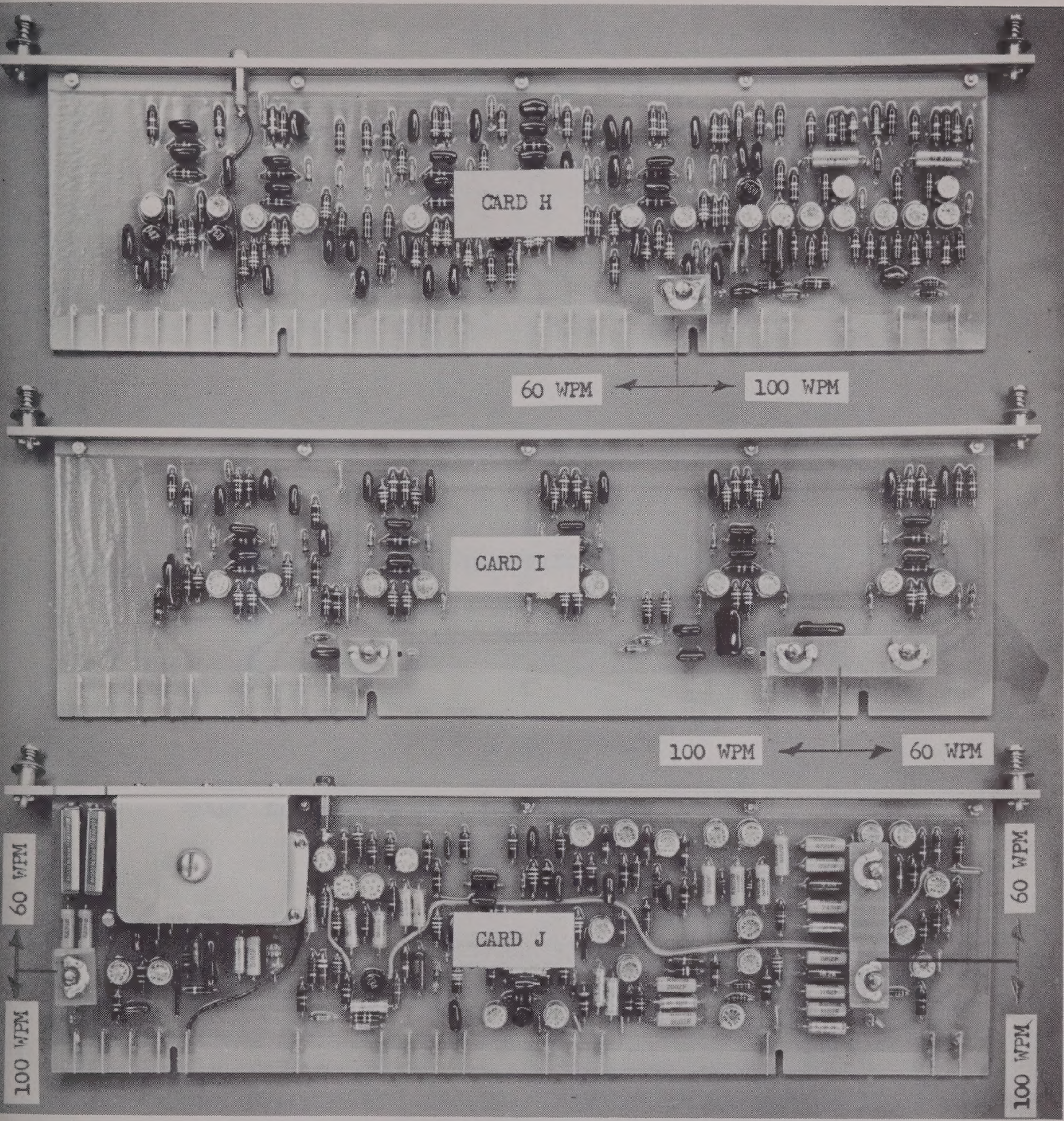

CARD H
60 WPM
100 WPM
CARD I
100 WPM
60 WPM
CARD J
60 WPM
100 WPM
60 WPM
100 WPM

FIG. 9. JUMPER POSITIONS ON SN-228(XC-2)/G CARDS (60 WPM POSITIONS SHOWN).

(PART II)

SERVICE TEST
INSTRUCTION MANUAL

SYNCHRONIZER, ELECTRICAL, SN-228(XC-1)/G

PART II. TECHNICAL INSTRUCTIONS

(PART II)

SYNCHRONIZER, ELECTRICAL SN-228(XC-2)/G

TECHNICAL INSTRUCTIONS

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CHAPTER 1

THEORY

Section I. GENERAL

1. Scope of Technical Instructions

a. The technical instructions cover stage by stage theory of operation and corrective maintenance data for the Synchronizer, Electrical, SN-228(XC-2)/G. Block diagrams, schematic diagrams, wiring diagrams, waveform diagrams, and trouble-shooting charts are included.

b. Installation and organizational maintenance for the SN-228(XC-2)/G are covered in Part I. Operating instructions are contained in KAO-86A/TSEC.

Note. In the following text, 60 wpm operation is assumed. One hundred wpm operation would be similar except all timing is shortened to approximately 60% of the 60 wpm value.

2. Block and Schematic Diagram Symbology

a. General. The theory of operation of the synchronizer is explained in the following section. A general theoretical description is given using a simplified block diagram (par. 3). The detailed theory (par. 4 through 29) is given using a complete logic block diagram, schematic, and timing diagrams.

b. Block Diagram Symbols. The detailed block diagram (fig. 2) displays all circuits of the synchronizer in symbolic form. The groups of symbols comprising each logic card are outlined and labeled with the card name and letter. Major circuits such as flip-flops (FF), and "AND" gates (G), and single-shots (SS) are numbered and correspond directly to the circuits on the schematic diagrams.

c. Schematic Diagrams. The schematic diagrams are divided as follows: one for each of the ten logic cards (A through J) (fig. 3 through 12), one for logic switches and relays (fig. 13), one for relay control circuits (fig. 14), and one for power supply (fig. 15). The circles with inscribed numbers, located on the schematic diagrams, represent the pins of the card connectors. When the pin of a particular card is referenced, the number is prefixed by a letter indicating the specific card, e.g., pin A-1 represents pin number 1 on card A. The letters and numbers adjacent to some connector pins represent the destination of the connection. For example, pin 8 of connector P1001 on card J (fig. 3), is indicated as being connected to card B-1, which represents pin 1 of connector P201 on card B (fig. 4).

Section II. BLOCK DIAGRAM AND SCHEMATIC DIAGRAM ANALYSIS

3. Simplified Block Diagram (fig. 1)

Each block consists of a group of transistor logic circuits. The general function of the blocks are related first in a sense which is common to both send and receive condition (a. below), second for the functions which occur only in the send condition (b. below), and third for the functions which occur only in the receive condition (c. below).

a. Common Functions. The character regenerator is the heart of the synchronizer. It generates a continuous stream of characters which operate the TSEC/KW-9 through the relay group when the start-stop control is in the start condition. The character regenerator rate of operation is accurately controlled by a tuning fork oscillator and binary divider (card B). Proper network phasing requires that a transmitting synchronizer and TSEC/KW-9 must phase lead each receiving synchronizer and TSEC/KW-9. The TSEC/KW-9 delay corrector advances the character regenerator in phase by a momentary speed-up when the synchronizer is switched to the send condition. The TSEC/KW-9 delay corrector retards the phase of the character regenerator by a momentary slow-down when the synchronizer is switched to the receive condition.

b. Send Functions. In the send condition, a TTY character from the KBD or TD enters the main signal integrator. This character is time-searched by the distributor and binary divider (card F). The distributor stores the five intelligence units of the input character in the extensor. This information is combined in a relay group with the blank character from the character regenerator. This intelligence character enters the TSEC/KW-9, is enciphered, and passed on to the radio transmitter by the output control. The output control does not allow the TSEC/KW-9 output to reach the radio transmitter unless the synchronizer receives an input character from TD or KBD.

c. Receive Functions. Each receiving synchronizer automatically phases its character regenerator on the TTY signals from a transmitting synchronizer. To perform this function, the TTY signal from the radio receiver enters the main signal integrator and is then passed to the extractor. The extractor tests the signal for a period of time, and if properly qualified, phases the character regenerator. The extractor is also operated by the distributor and binary divider (card F). After the character regenerator has been properly rephased, the received character is read out by the relay group and entered into the receiving TSEC/KW-9. If the incoming character was properly qualified, the output control passes the deciphered character to the TTY printer.

4. Detailed Block Diagram and Schematic Analysis

a. In paragraphs 5 through 29, detailed theory of operation of the individual cards, relay circuitry, and power supply is given. The detailed block diagram (fig. 2) referred to in each paragraph is used in the analysis.

b. In the following discussions the states of a flip-flop and single-shot multivibrator are referenced.

The terms used to describe these states are as follows: When the output is ground, the circuit is in the "one" or set condition; when the output is near -12 volts, the circuit is in the "zero"or reset condition.

5. Tuning Fork Oscillator (Card J)
(fig. 3)

a. The tuning fork and its associated amplifier circuitry form a regenerative system which oscillates at the fork's resonant frequency.

b. The signal from the tuning fork pickup coil (pin J-6) is amplified and fed back to the drive coil (pin J-7, fig. 17) by a highly stabilized, five-stage amplifier. Q1023 and Q1026 are used for impedance matching, and Q1024 and Q1025 are voltage amplifiers. A power amplifier Q1027 is connected to the tuning fork drive coil. The fork drive voltage is amplitude limited by zener diode CR1014. Fine adjustment of the fork frequency is made possible by series potentiometers R1089 for 60 wpm operation and R1088 for 100 wpm operation.

c. The output of stage Q1027 also drives a Schmitt trigger squaring circuit (Q1028 and Q1029) in which the fork oscillator output is shaped into a square wave with

50% duty cycle. A 2,000 cps tuning fork is used for 60 wpm operation, and a 3,260 cps tuning fork is used for 100 wpm operation. In the following text, 60 wpm operation is assumed.

d. The square wave output of the Schmitt trigger circuit (0.5 ms interval pulses) is made available at test jack J1011 and is also continuously applied to the binary divider and phase corrector (pins J-8 and B-1, par. 6a). Similar pulses of opposite phase are applied to another binary divider (pins j-9 and f-10, par. 9a) when gate G23 (CR1013) is open (par. 10c).

6. Binary Divider and Phase Corrector (Card B) (fig. 4)

a. A binary divider, FF10 through FF16, is used to step down the frequency of the tuning fork oscillator (par. 5). With no feedback, the output pulse interval of the binary divider is 32 ms with the 0.5 ms pulse interval from the oscillator, (pin B-1). Several feedback paths (pins B-10, B-9, and B-11) from the character regenerator and delay corrector (par. 21 and 22) are provided to make the output pulse interval 22 ms, 14 ms, or 9 ms.

b. The output pulse interval can be further modified by the action of FF9 and gate G10. The normal condition of FF9 is such that gate G10 is open, allowing the divider to operate normally (oscillator pulses are applied directly to FF10). If FF9 is triggered through pin B-2 (par. 16), closing gate G10, the output pulse interval of the divider can be lengthened by 0.5 ms. The next oscillator pulse cannot reach the divider but is connected to FF9, returning FF9 and gate G10 to their normal state. This action causes the divider to miss one 0.5 ms pulse and provides a slow retard function. A similar but longer interval (fast retard) of 4 ms is provided by FF13 and gate G11 which operates in the same manner as the slow retard circuit but connects to a later divider stage through pin B-6. The output pulse interval can be shortened by 0.5 ms (slow advance) and by 4 ms (fast advance) by a feedback pulse to FF10 (pin B-3) and FF14 (pin B-7), respectively (par. 16). Transmission delay correction is also accomplished manually through pins B-4 and B-5 and through DELAY CORRECTOR - OFF switch S2 (par. 20).

c. The output of the binary divider (pin B-14) is delayed about 20 μsec by SS1 to avoid coincidence of the feedback pulses and the main drive pulses from the tuning fork oscillator, and is applied to the character regenerator (par. 7) through pin B-14.

d. The output of FF15 is applied to gate G43 through pin B-8 (par. 23_d_.).

7. Character Regenerator (Card A)
(fig. 5)

_a_. The character regenerator is an eight station shift register connected as a ring counter with one circulating bit. One of the eight flip-flops, FF1 through FF8, is in the "one" state and all others are in the "zero" state at any given time. The binary divider output (par. 6) is connected to an input line (pin A-17) common to all ring counter stages. With each input pulse, the "one" state moves to the next stage, and so on around the ring.

_b_. FF1 through FF6 are each given a time interval of 22 ms by connecting each of the stages to the 22 ms feedback line of the binary divider (pin A-11). The connection is made through diode isolating gates ("OR" gates) to prohibit interaction between stages. FF7 and FF8 are given an interval of 14 ms each by similar connection to the 14 ms feedback line (pin A-12).

c. Addition of the time intervals of the individual stages totals 160 ms which is the length of the TTY character produced by the synchronizer. A BLANK character is obtained by letting the "one" state of FF1 represent the start baud and the "one" state of the FF7 and FF8 represent the stop baud. The "one" transition of FF1 is connected to the space input of FF51 (pin H-17), a signal mixing flip-flop (par. 24c.). The "one" transition of FF7 is connected to the mark input of FF51 (pin H-20). After amplification by relay driver transistors, the BLANK character is converted to a neutral 60 ma signal in TTY relay K1 (par. 28g.).

d. The "one" state of FF2 through FF6 provides the sampling pulses used to read the condition of the five intelligence bauds of the input signal in both transmit (par. 11) and receive (par. 17) modes. The time relationship of the signal at each stage is shown in figure 16.

8. Main Signal Integrator (Card J)
(fig. 3)

a. In the send mode of operation, the TTY input to the main signal integratoe is connected directly to a TTY KBD and/or TD. In the receive mode, contacts of relay K3 (par. 28h.) are introduced between the radio receiver/converter and input transistor Q1001.

b. Except for the signal source, the operation of the main signal integrator is the same in both send and receive modes. Low level switching is employed in the input to reduce radio interference. The base of the input transistor Q1001 (pin J-1) is grounded on mark (closed contacts). The maximum current switched is 550 µa and the maximum voltage is 2 volts. Q1001 through Q1003 are amplifiers used to increase the low switching current to a more usable value.

c. The remaining circuitry in the main signal integrator reduces the effect of noise in the incoming signal and squares the signal for use by the synchronizer.

(1) Q1004 and Q1005 are connected in complementary symmetry to provide a low driving impedance in both a positive and negative direction for the RC integrator circuit R1009 and C1001. The driving voltage for the integrator operates between zero volts for mark input and -12 volts for space input. The voltage across C1001 is clamped at -9 volts

during a space input and at -3 volts during a mark input. Since the capacitor charges toward -12 volts or discharges toward zero volts, the charge waveform within the bounds of the diode clamps is somewhat linear.

(2) Emitter followers Q1007 and Q1008 are used to present a high load impedance to the integrator circuit. The integrated output of Q1008 is connected to Schmitt trigger stage Q1009 and Q1010. The Schmitt trigger stage is biased by Q1006 so as to operate with very little hysteresis when the integrated voltage crosses -6 volts from either direction.

(3) The time constant of the integrator is such that an input signal must remain in one condition for at least 4 ms before the voltage across C1001 reaches -6 volts and operates the trigger circuit. This means that noise pulses with a duration shorter than 4 ms are effectively removed from the TTY signal during the time that bauds are sampled for information.

d. The output of the Schmitt trigger circuit varies between -12 volts and -6 volts. Amplifier Q1012 is used to transform the 6 volt signal to a signal operating between -12 volts and zero volts. Emitter follower Q1011 is used to provide a low impedance signal source in which mark is zero volts and space is -21 volts (pin J-5). This output is referred to as the MAIN SIGNAL. A main signal of the opposite polarity is provided by inverter Q1013. This output is known as MAIN SIGNAL INVERTED. The inverted polarity is -12 volts for mark and zero volts for space (pin J-12). The inverted output is also applied to flip-flop FF-45 (par. 10c. and d.) and to Q1016 (par. 25).

e. An etched circuit jumper (speed change jumper) is provided to change the RC integrator time constant for 100 wpm operation. The main signal time delay (c. (3) above) at 100 wpm is about 2.5 ms. Figure 17 is a timing diagram showing the integrator circuit and its effect on a noisy signal.

f. It is necessary that the input to the synchronizer be held on steady space for a short time after the send to receive switchover (par. 19). Q1028 and its associated circuitry perform this function. During the send mode, pin J-10 is ungrounded (due to opened contacts 8-D of relay K12 (par. 19)) and C1026 is discharged allowing Q1028 to be biased to cutoff. Q1028 in the cutoff condition has no effect on the incoming signal. When the synchronizer is switched to receive, pin J-10 is grounded through contacts 8-D of relay K8, forcing C1026 to charge through the base-emitter junction of Q1028. The charging current amplified by Q1028 produces a voltage drop in R1003 causing the base of Q1002 to drop to zero volts, which is the space condition. When C1026 becomes fully charged, the current through Q1028 ceases and the circuit no longer affects the TTY signal input. The time constant of the RC charge path is such that the main signal is held in the space condition for approximately 0.8 second after each transmit-receive switchover (par. 19).

9. Binary Divider, Send Mode, (Card F)
(fig. 6)

a. The six stage binary divider, FF23 through FF28, receives 0.5 ms interval pulses from the fork oscillator Schmitt trigger circuit (pin F-10) when gate G23 is open (par. 10 c.). These pulses are taken from the collector opposite the one used to drive the character regenerator section (par. 5). Since the Schmitt trigger output is a 50% square wave, this opposite phase produces an interlacing of trigger pulses and prohibits a coincidence of signals from the character regenerator and the extensor (par. 11). The binary divider has a normal output interval of 32 ms with no feedback applied. A feedback path is provided from the distributor through pin F-2 and contacts F-11 of relay K11 (fig. 13) to make the output interval 22 ms. The output of the binary divider (pin F-7) to the distributor (par. 10) is delayed about 20 µsec by SS4 to avoid coincidence of the feedback pulses and the main drive pulses.

10. Distributor, Send Mode, (Card C) (fig. 7)

a. The distributor is a five stage shift register connected as a ring counter and driven by the binary divider (par. 9). The "one" condition circulates stage by stage with each input pulse to pin C-7.

b. FF17 through FF20 are given an interval of 22 ms by "OR" gate feedback through pin C-15 and contacts F-11 of relay K11 to the 22 ms feedback loop on the binary divider. FF21 has an interval of 32 ms since it has no feedback connection.

c. The purpose of the distributor is to read the information in the input signal bauds. It does not run continuously but is started at the beginning of an input character and stopped after readout is finished. This function is performed by FF45 (Q1014 and Q1015) and its associated "AND" gate G23 (CR1013), which is introduced between the oscillator trigger circuit and the binary divider (fig. 3). With no TTY input, the normal state of the distributor is FF21 in the "one" condition and FF45 in the "zero" condition, holding gate G23 closed. With the gate closed, the distributor remains idle.

d. One input of FF45 is connected to the main signal (par. 8d.). When the main signal integrator receives an input character from a KBD or TD, FF45 receives the positive transition of the start baud and switches to the "one" condition, opening gate G23. The bit remains in FF21 for 32 ms and then moves to FF17 through FF20 in 22 ms intervals. Figure 18 shows the time relationship between the incoming signal and the distributor operation. The transitions from the "zero" to the "one" state of the distributor stages are located near the center of the bauds of the incoming main signal and are used as sampling pulses in the input to the extensor storage system (par. 11b.). When the bit returns to FF21 the "one" pulse (pin C-11) resets FF45 and gate G23 to the normal (closed) condition. The distributor then remains idle until another input character begins. FF22 (par. 14) is disconnected and disabled by relay K12 in the send mode (pin C-12). SS8 functions in the send-receive switchover (par. 27d.).

11. Extensor (Card D)
(fig. 8)

a. The extensor is used in the send mode of operation. The extensor stores the non-synchronous input character for synchronous readout by the character regenerator.

b. The main signal (par. 8d.) input (pin D-16) controls AND gates G38 through G42 which are open during mark signals and closed during space signals. Sampling pulses from the distributor (par. 10d.) also appear on gates G38 through G42 on pins D-1, D-3, D-5, D-7, and D-9, respectively. If the first baud appears as a mark, then gate G38 will pass the sampling pulse to storage FF29 setting it to the "one" condition. In this condition, FF29 opens mark gate G13 and closes space gate G14.

c. Synchronous sampling is done by the "one" transitions of the character regenerator flip-flops FF2 through FF6 representing the regenerated intelligence bauds 1 through 5, respectively (par. 7). These sampling pulses appear at pins D-2, D-4, D-6, D-8, and D-10. When the first baud mark gate G13 is opened (b. above), the sampling pulse is passed through pin D-11 and contacts 9-E of relay K12 to H-19 which is the mark input of FF51 (fig. 19). Space gate G14, being closed, does not pass a pulse to FF51. The sampling pulse received by gates G13 and G14 is also used to reset storage FF29 back to the "zero" state. Mark gate G13 closes and space gate G14 opens, passing the sampling pulse to FF51 space input through contacts 11-F of relay K12. The storage and readout of bauds 2, 3, 4, and 5, is identical, except that extensor stages FF30 through FF33 and mark and space gates G15 through G22 are involved.

d. The TD input (pin D-16) to the extensor has a normal character length of 163 ms. Since the regenerated character is 160 ms long, there is a phase drift between the input signal and the regenerated signal. This causes a speed differential blank character approximately every 53 characters, which is normal.

12. Output Control, Send Mode, (Card G) (fig. 9)

a. With no input signal, the synchronizer in the start mode runs the TSEC/KW-9 continuously. An output control circuit is used to allow only input intelligence characters to reach the transmitter/modulator.

b. If FF47 receives no pulse from the distributor (pin G-5), it remains in the "one" state. The output control relay, K5, remains de-energized through pin G-15 holding the transmitter/modulator on steady mark. When an input signal starts the distributor (par. 11), FF47 is triggered to the "zero" condition and later back to the "one" condition by FF5 of the character regenerator. The "one" transition triggers SS5. SS5 has a 20 μsec delay used to prevent pulse coincidence in FF48. After this delay, FF48 is triggered to the "one" condition. Q709 and Q710 are current amplifiers used to energize relay K5 (fig. 14). K5 then switches the TSEC/KW-9 output character to the transmitter/modulator. FF48 receives a pulse from FF5 160 ms later and returns to the "zero" state, de-energizing relay K5.

c. The output control is triggered by FF5 of the character regenerator because its "one" transition occurs at 110 ms, as shown in figure 20. This allows the output control and relay K5 to be fully operated before 124 ms, the time delay through the TSEC/KW-9. During TD transmission, relay K5 remains closed between characters except during the speed differential blank character.

13. Binary Divider, Receive Mode, (Card F) (fig. 6)

In the receive mode, the binary divider receives 0.5 ms interval pulses (pin F-10) continuously. The normal output interval (pin F-7) with no feedback is 32 ms. Three modified output intervals are provided. Feedback to pins F-1, F-2, and F-3 cause output intervals of 27 ms, 22 ms, and 10 ms, respectively. A pulse on the reset line (pin F-4) resets all stages to the "zero" condition.

14. Distributor, Receive Mode, (Card C) (fig. 7)

In the receive mode, FF22 is used (through contacts B-3 and A-1 of relay K12) changing the distributor to a six stage ring counter. The common input line (pin C-7) receives drive pulses from the binary divider (par. 13). FF17 is given an interval of 27 ms by connection through pin C-4, contacts A-1 of relay K11, and pin F-1, which is the 27 ms feedback line of the binary divider. FF18 through FF21 have 32 ms intervals since there are no feedback connections. The normal interval of FF22 is 10 ms with no received signal. The 10 ms feedback connection is through pin C-13 to pin F-3 of the binary divider. The total time interval for all stages is 165 ms.

15. Extractor, (Card E)
(fig. 10)

a. The extractor, in conjunction with the distributor, is used in the receive mode to search an incoming TTY signal and find the stop to start transition. The extractor samples this transition continuously. If this transition appears eight times in succession, the extractor gates this information to the character regenerator for phasing purposes.

b. The 10 ms "one" interval of distributor FF22 (par. 14) enters the extractor at pin E-1 and feeds a load isolating emitter follower Q501. The output of Q501 controls gate G24. The other gate input (pin E-2) is the inverted main signal (par 8d.).

c. The normal distributor period is 165 ms and a synchronous received signal period is 160 ms. The 10 ms distributor pulse therefore drifts 5 ms each cycle with respect to the received signal. During 10 ms each character, when gate G24 is open, a mark to space main signal transition will trigger SS2. The triggering of SS2 indicates the possibility of a stop to start transition. The distributor begins to operate at the same rate as the main signal in the following manner. SS2 output pulse is fed through pin E-5 to divider pin F-4 which is the divider reset line (par. 13). Resetting of the divider allows another distributor cycle to start immediately. As long as SS2 pulse is present, the distributor is forced to run at 160 ms in step with the received signal. Since the distributor is now 160 ms, the former 10 ms gating pulse is shortened to 5 ms. The end of the 5 ms pulse is coincident with the received mark to space transition.

d. Intelligence baud mark to space transitions or even random noise transitions will trigger SS2 if they are coincident with the 10 ms gating interval. However, only the stop to start transition will occur every character and at the same time each character. The pulse from SS2 enters a four stage counter, flip-flops FF41 through FF44. After eight input pulses to the counter, the "one" condition reaches FF44 opening gate G27. The stop to start transition pulse passes through gate G27 (pin E-6) to the character regenerator phasing circuits (par. 16). If SS2 does not experience eight successive transitions, the counter is reset to zero and gate G27 remains closed.

_e_. SS3 initiates the reset circuitry. When no mark to space transition passes through gate G24, SS3 receives no trigger from SS2 and remains in its stable state. The collector of Q505 is at -12 volts causing the emitter of gating transistor Q506 (gate G26) to follow at -12 volts. The conduction through R516, CR504, and R518 holds the junction of CR504 and R518 at about +2 volts. The negative trailing edge of the 10 ms pulse is coupled through capacitor C511 to the junction of CR504 and R518. This negative pulse reverse biases CR504 causing the current through Q506 to flow through R516, CR505, and the base of Q509. Q509 is a reset driver and, when biased to conduction, resets the counter to "zero". If SS2 does not experience a mark to space transition, FF22 runs its full interval of 10 ms causing the extractor to search 5 ms per character once again.

f. If a large amount of random noise is present in the main signal, the extractor might falsely qualify the noise. If more than one mark to space transition of the main signal occurs within the 10 ms gating interval, random noise is assumed and the counter is reset. The circuitry associated with FF40 resets the counter in case of more than one transition. One input to FF40 comes from SS2. A pulse here indicates one mark to space transition and switches FF40 to the "one" condition opening gate G25. Gate G25 is similar in operation to gate G26 (e. above). Another input to FF40 (pin E-4) comes 11 ms later from FF28 of the binary divider (card F). This pulse returns FF40 to the "zero" state closing gate G25. Another input to gate G25 is the main signal. If a mark to space transition occurs in the main signal while gate G25 is open, indicating more than one transition in the sampling period, Q509 conducts and resets the counter to zero.

16. Character Regenerator Phasing, Receive Mode, (Card A) (fig. 5)

a. After the extractor qualifies the received stop to start transition, the character regenerator is caused to align its phase to properly sample incoming baud information. This phase alignment is shown in figure 16. The leading edge of the "one" pulse of FF8 must align with the extractor pulse from gate G27 for proper phasing (par. 15d.). Gates G1 through G8 are controlled by flip-flops FF1 through FF8, respectively, of the character regenerator.

b. A common line input to the gates receives the extractor pulse (pin A-22). The common output of gates G1, G2, and G3, is the fast retard feedback pulse (pin A-21). The output of gate G8 is the slow retard feedback pulse (pin A-20). The common output of gates G4, G5, and G6, is the fast advance feedback pulse (pin A-19). The output of gate G7 is the slow advance feedback pulse (pin A-18).

c. If the extractor pulse (pin A-22) occurs coincident with the "one" condition of flip-flops FF4, FF5, or FF6, then gate G4, G5, or G6 is open and the pulse is connected through pins A-19 and B-7 to the fast advance input of the binary divider (par. 6). The binary divider output interval is shortened 4 ms thus shortening the character regenerator interval to 156 ms. The character regenerator advances in phase 4 ms each character and approaches the correct phase relationship. If the extractor pulse first appeared in coincidence with FF4, the advance would cause the pulse to become coincident with FF5 and later FF6. When the pulse passes out of the FF6 region, it becomes coincident with FF7 "one" condition. Gate G7 is connected through pins A-18 and B-3 to the slow advance input. The binary divider output interval now shortens by 0.5 ms each character. The character regenerator continues to advance at a slower rate of 0.5 ms per character.

d. Similarly, if the extractor pulse (pin A-22) occurs coincident with the output of the flip-flops FF1, FF2, or FF3, the character regenerator is retarded in phase 4 ms each character until pulse coincidence reaches FF8. The fast retard pulse goes through pins A-21 and B-6 to the binary divider FF13. When the extractor pulse becomes coincident with the "one" condition of FF8, the slow retard gate G8 output (pins A-20 and B-2) continues to retard the character regenerator at a 0.5 ms per character rate.

e. When the pulse passes out of the FF7 region and into the FF8 region, coincidence occurs in gate G8. The character regenerator will then retard in phase by 0.5 ms. This resultant alternate advancing and retarding is a servo-type hunting around the correct phasing point, which is the transition between FF7 and FF8. Figure 23 shows the correct phase relationship between an incoming signal and the character regenerator.

17. Received Signal Readout, (Card G) (fig. 9)

After the character regenerator phasing is completed, (par 16), the synchronizer is prepared for baud sampling of the main received signal. This is done in gates G30 and G31. A common input (pin G-20) to both gates is five pulses from FF2 through FF6 which are the sampling pulses for the five bauds. The control input to gate G30 is the main signal inverted (par. 8d.), which opens the gate during a space signal. The control input to gate G31 is the main signal which opens the gate during a mark signal. The five bauds in a received signal are sampled serially. The mark and space lines from gates G31 and G30 go through contacts 10-E and 12F respectively of relay K12 to pins H-19, and H-16 (fig. 12) which are the appropriate inputs of FF51. FF51 operates TTY relay K1 through driver stages Q820 and Q822.

18. Output Control, Receive Mode, (Card G) (fig. 9)

a. The output control is used in receive to hold the page printer on steady mark when there is no input character. Gates G28 and G29 sample the main signal for the presence of a stop and start baud.

b. If the "one" condition of FF7 (pin G-7) is coincident with a main signal mark (pin G-3), gate G29 triggers FF46 to the "zero" condition. If, 28 ms later, the "zero" transition of FF8 (pin G-1) is coincident with a main signal inverted space (pin G-2), gate G28 triggers FF46 back to the "one" condition. The "one" transition of FF46 triggers FF47 to the "zero" condition through contacts 3-B of relay K11. FF47 receives its next pulse from FF5 through pin G-6 and switches to the "one" condition. The "one" transition of FF47 is passed through SS5 to FF48. This operates relay drivers Q709 and Q710, energizing relay K6 (fig. 14). Relay K6 switches the printer from steady mark to the TSEC/KW-9 loop output character.

c. The pulse from FF5 accounts for the character delay through the TSEC/KW-9 and assures that switching is performed at a safe time during the stop baud. A timing diagram is shown in figure 22. The next pulse from FF5, 160 ms later, triggers FF48 back to the "zero" condition, de-energizing relay K6.

19. Send-Receive Switching (Card G) (fig. 9)

a. The synchronizer send-receive switching in the logic circuits is done by relays K11 and K12 (fig. 13). The time of switchover to send occurs when pin G-8 is grounded through contacts 6-7 of relay K7 (fig. 14) which operates when S1 is in SEND position. This opens a gate (CR714) allowing FF7 pulse (fig. 5) to trigger FF39 through Q808 (fig. 12). When FF39 switches to the "one" condition, the collector of Q715 goes to -12 volts, biasing relay drivers Q717, Q718, and Q719 on. Q719 provides current to energize relays K11 and K12 (fig. 13)

b. Receive switchover occurs when S1 is in RECEIVE position and pin G-9 is grounded through contacts 7-C of relay K7 (fig. 14). This opens a gate (CR715) allowing

FF7 pulse to trigger FF39 (a. above). When FF39 switches to the "zero" condition, it biases the relay drivers to cut-off, de-energizing K11 and K12 relays.

20. Transmission Delay Correction (Card G) (fig. 9)

SS9, SS10 and associated circuitry are used to partially correct for the added signal delay caused by a long distance radio link. SS9 is triggered by FF39 at send switchover (par. 19). The outputs of either SS9 and SS10 are fed through S2 in the DELAY CORRECTOR position (fig. 13) to the binary divider FF14 (pin B-5) and FF13 (pin B-4), respectively (fig. 4). When the DELAY CORRECTOR-OFF switch S2 is in the DELAY CORRECTOR position, a pulse from SS9 at send switchover advances the binary divider and character regenerator 4 ms (par. 6 and 7). At receive switchover, a pulse from SS10 retards the character regenerator 4 ms, returning it to its original phase.

21. Delay Corrector, Send Mode, (Card I) (fig. 11)

a. When switched to send, the character regenerator must be advanced in phase so that the signal sent to the receiving synchronizer is phased correctly. The advance must be 150 ms due to the 124 ms delay through the TSEC/KW-9 plus 26 ms of delay by various other circuit functions. Figure 23 shows the phase relationship at the character regenerator of transmitting and receiving synchronizers.

b. At send switchover, the "one" transition of FF39 (par. 19) (G-11) triggers FF38 (I-4) to the "one" condition, opening gate G-12. The "one" pulses from FF7 and FF8 (through pin I-6) pass through gate G-12 to the binary divider 5 ms feedback line (pin B-11). The two feedback pulses shorten the interval of FF7 and FF8 by 5 ms each, making the character length 150 ms.

c. A binary divider, FF34 through FF37, determines the number of times the character regenerator is allowed to advance. The input to the binary divider (pin I-7) comes from the FF7 and is controlled by FF38 and gate G9. The output of the binary divider is used to reset FF38 back to the "zero" condition. The "zero" condition of FF38 closes gates G-9 and G-12, stopping the advance. At the beginning of the advance cycle, the "one" transition of FF39 sets the divider, by feedback connections, for a count of 15. The controlling gates G-9 and G-12 are open for fifteen

10 ms intervals totaling the necessary 150 ms advance.

22. Delay Corrector, Receive Mode, (Card I) (fig. 11)

a. At receive switchover, the character regenerator phase must be retarded 150 ms to its original phase.

b. Due to an inherent function of the TSEC/KW-9, a send to receive switchover causes the TSEC/KW-9 to pause for one character, thus effectively retarding the synchronizer 160 ms. It is necessary then to advance 10 ms to arrive at the original phase. The same circuitry is used for the 10 ms advance as for the 150 ms advance (par. 21). The only difference is that the divider is set for a count of one by the operation of FF39.

c. A manual advance feature is provided by S6 (fig. 13) and gate G46 (pin I-1). Closure of S6 opens gate G-46 allowing FF7 (pin I-7) to trigger FF38 starting an advance cycle. The four stage divider (FF34 through FF37) runs for its full count of 16, giving a full character advance of 160 ms. Switch S6 also provides a manual retard feature (par. 27a.).

23. Special Character (Card H)
(fig. 12)

a. A special character which approximates the TTY letter "M" is generated and transmitted for 12 seconds to initially phase all synchronizers. The special character is also initiated automatically at the beginning of each transmission.

b. SS7 is a special 12 second monostable multivibrator made up of Q801, Q802, and Q803 and is the timer for special character transmission. SS7 can be manually triggered through pin H-2 and contacts D-7 of relay K11 by SPECIAL CHARACTER switch S3 (fig 13). SS7 is also triggered automatically at each send switchover through pin H-3 and contacts 6-C relay K11 from the output of the delay corrector binary divider FF37 (pin 12) (par. 21). The trigger is taken from FF37 so that the special character is not initiated until the character regenerator has advanced 150 ms. The automatic special character can be disabled by changing a jumper connected to pin I-2.

c. When SS7 is triggered to the "one" condition, gate G37 is opened by gate driver Q804. Gate G37 controls the space input of FF52 which is the special character mixing flip-flop. Gate G36, which is normally open, controls the mark input of FF52.

d. The space input to gate G37 (pin H-8) comes from a coincidence in gate G43 (fig. 5) of the "one" condition of FF6 (par. 7) and a zero pulse from FF15 (par. 6). This time corresponds with the time of the TSEC/KW-9 output stop to start transition.

e. The mark input to gate G36 (pin H-10) comes from FF3 (fig. 5). These mark and space inputs drive FF52 which operates TTY relay K2 through current amplifiers Q813 and Q816. The special character TTY signal at K2 is applied to the radio transmitter/modulator. At the end of 12 seconds, SS7 returns to its stable "zero" condition. Gate G37 closes and FF52 returns to its normal steady mark condition.

24. Start-Stop, Send Mode, (Card H)
(fig. 12)

a. A sending synchronizer provides a start signal which can be recognized and acted upon by a receiving synchronizer operator. This takes the form of a steady SPACE signal transmitted for an 8 second interval. At the end of this interval, sending and receiving TSEC/KW-9's begin operating automatically and in synchronism.

b. While S5 (fig. 13) is in the STOP position, FF50 is in the "zero" condition holding gate G35 closed. FF51 therefore remains on steady MARK and the TSEC/KW-9 does not operate. When S5 (fig. 13) is operated to START position, SS6 is triggered (pin H-5) to the "one" condition opening gate G-33 and closing gate G34 through gate drivers Q812 and Q811. SS6 is similar to SS7 (par. 23b.) except its running time is 8 seconds. FF7 in the character regenerator (par. 7) provides a pulse input through pin H-1 and Q808 to gates G33 and G34. The output of gate G33 triggers FF49 to the "one" condition, opening space gate G37 and closing mark gate G36. FF52 is triggered to SPACE by the output of gate G37 and remains in that condition. The space condition of FF52 causes a steady SPACE signal to be transmitted. At the end of 8 seconds SS6 returns to its "zero" condition, closing gate G33 and opening gate G34. The output of gate G34 returns FF49 to the "zero" condition, opening mark gate G36 and closing space gate G37. FF52 is triggered to the MARK condition returning the transmitted signal to steady MARK.

c. The START position of S5 also connects the start input of FF50 (pin H-14) through contacts E-9 of relay K11 to one output of FF49 (pin H-9). When FF49 returns to the "zero" condition, it triggers FF50 to the "one" condition. This opens space gate G35 and allows a blank character (par. 7c.) to reach FF51 through contacts F-12 of relay K12 and the extensor (par. 11). This causes the TSEC/KW-9 to begin operation.

d. When S5 is operated to the STOP position, SS6 is triggered and a steady SPACE is transmitted for 8 seconds by the same process described for starting (b. above). However, in the STOP position FF49 output is connected through S5 and contacts 9-E of relay K11 to the stop input of FF50 (pin H-15). At the end of 8 seconds, the "zero" transition of FF49 returns FF50 back to the "zero" condition. The "zero" condition of FF50 closes gate G35 and FF51 returns to steady MARK stopping the TSEC/KW-9.

25. Mark Integrator, Receive Mode, (Card J) (fig. 3)

a. A received start command is 8 seconds of steady space (par. 24) which a receiving synchronizer must indicate. During this time, the receiving operator must change the START-STOP switch S5 (fig. 13) to START to prepare the circuitry for receipt of the start pulse. The return of MARK at the end of 8 seconds of SPACE is the pulse used to start the TSEC/KW-9.

b. Visual indication and considerable noise immunity for the received stop-start command are provided by the mark integrator circuitry on card J. When the received signal is more than 50% mark, the indicator lamp I2 flashes at character rate. The base of integrator driver Q1016 receives a -11 volt potential from the main signal inverted output (pin J-12) when the received signal is steady MARK. The emitter of Q1016 follows, causing C1010 to charge toward -11 volts through CR1008 and R1041. The time constant is such that 90 ms of mark is required for the voltage to reach sensing diode CR1010. The anode of CR1010 is at -6 volts and when the voltage across C1010 reaches -6 volts, CR1010 starts to conduct. Current through CR1010 flows through the base-emitter junction of amplifier Q1019. The output of Q1019 triggers a monostable multivibrator Q1020, and Q1021, to the "one" condition. This multivibrator has an interval of slightly more than one-half character. The "one" condition of the multivibrator biases the lamp driver Q1022 such that the indicator lamp I2 goes off. Indicator I2 goes on again when the single-shot returns to the stable condition. The integrator capacitor C1010 is discharged once each character by amplifiers Q1017 and Q1018 which are driven by FF7 (pin J-2).

c. When the input signal is steady SPACE, as in a start command, integrator R1041 and C1010 receives no drive voltage. The single-shot does not receive a trigger and the indicator lamp stays on. When the input returns to steady MARK, the integrator charges to the sensing point and the single-shot is triggered. The "one" output opens gate G-32 in the start-stop circuitry (par. 26c.).

d. Since a total of 90 ms of MARK signal in any one character is required to open gate G32, considerable noise immunity is attained.

26. Start-Stop, Receive Mode, (Card H) (fig. 12)

a. The circuit is designed so that the receiving TSEC/KW-9 starts and stops in proper phase and character synchronism with the transmitting TSEC/KW-9.

b. With switch S5 (fig. 13) in the STOP position, FF50 is in the "zero" condition holding gate G35 closed. FF51 stays in the MARK position and the TSEC/KW-9 receives a steady MARK signal.

c. When the receiving operator sees the signal indicator lamp change from flashing to steadily on for 8 seconds, a start command (steady space) has been initiated by the transmitting operator (par. 24b.). During the 8 seconds, the START-STOP switch S5 is changed to the START position. Switch S5 connects the start input of FF50 (pin H-14) to the output of gate G32 through contacts 10-E of relay K11. The pulse input to gate G32 comes from FF7 (par. 7) and through pin H-1 and Q808. When the input signal returns to steady MARK, the mark integrator opens gate G32 (pin H-7). The next pulse from FF7 triggers FF50 to the "one" condition, opening gate G35 which allows FF51 and the TSEC/KW-9 to start operating on the next start baud (par. 24c.)

d. A similar procedure is followed in the stop command, except that S5 is changed to STOP position. In STOP position, the output of gate G32 triggers FF50 back to the "zero" condition. This closes gate G35 and stops the input signal to FF51. The TSEC/KW-9 ceases operation.

27. Miscellaneous Circuitry

a. Manual Retard (Card H), (fig. 12). A manual retard function is provided which allows the TSEC/KW-9 operation to be retarded one character at a time. When ADVANCE-RETARD switch S6 (fig. 13) is changed to RETARD position, FF53 is triggered to the "one" condition. This opens gates G44 and G45. The pulse input to gate G45 comes from FF8 (pin H-24) and triggers FF50 closing gate G35. The pulse input to gate G44 comes from FF7 (pin H-20) 145 ms later and triggers FF50 back to the "one" condition opening gate G35. Each time S6 is changed to RETARD, gate G35 is closed for one character and the TSEC/KW-9 pauses for that character.

b. CHECK-NORMAL Switch (fig. 13). The CHECK-NORMAL switch energizes the output control relay K6 (pin G-15) when the synchronizer is in the stop mode. This enables the printer to operate, affording a TSEC/KW-9 "letters" check.

c. Main Reset (Card D), (fig. 8). A diode isolated reset line is connected to each stage of the character regenerator and the distributor. This assures the proper condition of all stages when the power is applied. Additional lines trigger FF38 and FF50 to their "zero" condition. When the power supply is turned on (par. 29), the negative supply line rises toward -12 volts. This change is coupled to the base of reset driver Q401 through R403 and C402. The base current causes the collector of Q401 to remain at zero volts until C402 charge current ceases. The collector and the reset line connected to it (pins D-17 and D-18) then go to -12 volts and are isolated by diodes from the flip-flops that were reset.

d. Send-Receive Reset (Card C), (fig. 7). SS8 is triggered through contacts C-6 and C-5 of relay K12 at each send or receive switchover. The output of SS8 resets the distributor and FF45 to assure the proper condition of the circuits.

28. Input-Output Circuits

a. General (fig. 14). The radio equipment, TTY equipment, TSEC/KW-9, remote control box, and logic circuitry of the synchronizer are connected together through a group of relays (c. below) and connectors (b. below). Feed-through capacitors (C1 through C9) in the logic circuitry which feed the input-output circuits are located on the left side of figure 14. Input-output relay control circuitry is described in d. through i. below.

b. Connectors. The chart below lists the connectors and their functions.

Connector	Function
J1	Connector for remote control cable which provides send-receive switchover in the radio set through operation of the SEND-MARK HOLD-RECEIVE switch S1 in the synchronizer.
J2	Connector for remote control box which controls send-receive and plain-cipher switchover for the synchronizer.
J3	Connector for cable which goes to the radio receiver/converter.
J4	Connector for the cable which goes to the radio transmitter/modulator.
J5	Connector for the cable which goes to the TSEC/KW-9.
J6, J7	Phone jacks which accept plugs from the teletypewriter keyboard or TD.
J8, J9	Phone jacks which accept plugs from the teletypewriter printer or reperforator.
J10	Phone jack which accepts plug from a teletypewriter TD for security interlock.

c. Relays. The chart below lists the input-output relays and their functions.

Relay	Function
K1	TTY polar relay. It is operated by flip-flop FF51 of the logic circuit and provides the main signal to the TSEC/KW-9.
K2	TTY polar relay. It is operated by flip-flop FF52 of the logic circuit and provides the special character and the start and stop command signals to the radio transmitter.
K3	TTY polar relay. In cipher receive, it is operated by the radio receiver and provides the main signal into the synchronizer. In plain send, it is operated by the keyboard or TD and it provides a security interlock.
K4	Miniature telephone type hermetically sealed relay. This is operated by flip-flop FF39 with driver (par. 19) and provides the send-receive switchover for the TSEC/KW-9. It assures that the synchronizer signal enters the TSEC/KW-9 loop circuits in send and TSEC/KW-9 line cir-

c. Relays. (Con't.).

Relay	Function
	cuits in receive. This relay also selects output controls.
K5	Miniature telephone type relay hermetically sealed with K6. This relay is operated by flip-flop FF48 of the output control in the send mode (par. 12). It holds the transmitter on steady MARK while the TSEC/KW-9 is enciphering blanks. It connects the transmitter to TSEC/KW-9 output when valid information occurs.
K6	Miniature telephone type relay hermetically sealed with K5. This is operated by flip-flop FF48 of the output control in receive. It holds the printer on MARK during periods of deciphering garble and connects the TSEC/KW-9 output to the teleprinter when valid information occurs.
K7	Miniature telephone type relay hermetically sealed with K8. It is operated when SEND-MARK HOLD-RECEIVE switch S1 is in the SEND position. It switches the teleprinter and radio receiver in

c. Relays (Con't.).

Relay	Function
	plain text. It initiates send-receive switchover for the logic circuits and operates in the security interlock system.
K8	Miniature telephone type relay hermetically sealed with K7. This is a high impedance, high voltage relay and controls the security interlock circuit during plain send operation. In conjunction with C10, R2, and R3, it provides an 8 second, 4 second, or 2 second security time option (par. 28c.).
K9, K10	Miniature telephone type relays separately hermetically sealed. These relays are operated when P-C switch S4 on the remote control box and the P-C switch on the TSEC/KW-9 are in C position. They provide all the plain-cipher switching required in the synchronizer and radio set.

d. Input-output Control Circuits, General. The control circuit is described in the following functional breakdown: Plain send; plain receive; cipher send; and cipher receive.

Figures 24 through 27 show the simplified circuits of these four functions. Each circuit begins at ground, follows through all involved components, and ends at a power supply potential.

e. Plain Send Mode.

(1) In the plain send mode (fig. 24), two separate circuits are involved. The first circuit connects the KBD and TD, TTY relay K3, printer, and radio set transmitter in one series circuit to the TTY loop supply potential of +130 v dc. A security interlock contact bypasses the KBD and TD input ((2) below).

(2) The second circuit is the security interlock itself. This is a timing circuit consisting of the relay K8 coil, capacitor and resistor in parallel connected to 130 volts (fig. 14). After PLAIN-START switch S9 is actuated, the circuit is kept charged by the switching action of TTY relay K3 through contacts 5-6 of relay K8, maintaining the interlock open. If relay K3 does not close during a selected period of time due to no transmission from the KBD and TD, the security interlock cir-

cuit will short circuit the KBD and TD contacts through contacts 2-3 of relay K8.

(3) When only capacitor C10 is in parallel with the winding of relay K8 (resistors R2 and R3 disconnected), the security interlock time interval is 8 seconds. When capacitor C10 and only resistor R3 are connected in parallel, the security interlock time interval is 4 seconds. When the capacitor and only resistor R2 are connected in parallel, the secutity interlock time interval is 2 seconds.

f. Plain Receive Mode. In the plain receive mode (fig. 25) one circuit is used. This is a series circuit consisting of the radio receiver, printer, loop resistor, and TTY loop supply potential of +130 v dc.

g. Cipher Send Mode. In the cipher send mode (fig. 26), five separate circuits are involved. The TSEC/KW-9 loop input is provided by the TTY signal from relay K1. The TSEC/KW-9 line hold is required to prevent a line break within the TSEC/KW-9. The radio transmitter circuit is selected by the transfer contacts of relay K5. With no information input, the transmitter is connected to the special character TTY relay K2. For valid information input, the transmitter is connected to the line output of the TSEC/KW-9 (connector J5). In the synchronizer input circuit, the KBD and TD are connected to feed-through C9 which goes to the main signal integrator (par. 8). In the home copy circuit, the printer is connected to the TSEC/KW-9 loop circuits.

h. Cipher Receive Mode. In cipher receive mode (fig. 27), five circuits are involved. In the radio receiver circuit, contacts from the receiver, TTY relay coil, K3, and loop resistor R15, are connected to the TTY loop supply. In the synchronizer input circuit, TTY relay K3 provides a signal to the main signal integrator. In the TSEC/KW-9 line input circuit, TTY relay K1 provides a signal to the TSEC/KW-9 line. A TSEC/KW-9 loop holding circuit is provided. In the printer circuit, transfer contacts on relay K6 are connected to the printer. With no valid information input, the printer is held on a TTY loop supply or steady mark. With valid information input, relay K6 transfers the printer to the TSEC/KW-9 loop output.

i. Radio Connection Strip. The connection strip provides various power input and output options for the radio equipment. Allowable options are given in paragraphs 12, 13, and 14, Part I of this manual. The connection strip in figure 14 is shown connected for use with the AN/GRC-46 radio set.

29. Power Supply and Tuning Fork Oven (fig. 15)

a. The power supply furnishes unregulated negative 24 volts; regulated negative 12 volts; regulated positive 6 volts; and unregulated positive 130 volts.

b. When ON-OFF switch S8 is in position ON, 115 v ac at 50 to 60 cps is applied to primary winding 1-3 of transformer T1. AC POWER lamp I1 lights, indicating the application of power. The primary voltage source bypasses switch S8 and is directly applied to the tuning fork oven when plug P11 is connected to the 115 v ac source.

c. The three rectifier systems use full wave rectification with center-tapped transformed windings. The filtered output of the negative 24 volt supply is obtained from secondary winding 5-7 and is used for operating relays and certain indicator lamps. The negative 12 volt output is taken across a zener diode shunt regulator (CR9) fed from the 24 volt supply. The 12 volt supply is used to power all the transistor circuitry. The positive 6 volt supply, used for biasing, is taken across a zener diode shunt regulator (CR10) whose input is approximately 12 volts from transformer winding 11-13. Transformer winding 8-10 furnishes a nominal 130 volts unregulated used for supplying the teletype loop current.

d. The primary circuit of the power supply is protected by 1.5 A SB (slow-blow)-ac fuse F1. The positive 130 volt output circuit is protected by .5 A SB-TTY fuse F2 .

e. The heater element (HR1) of the tuning fork oven is connected to the primary ac line bypassing power ON-OFF switch S8. This heater in conjunction with mercury thermostat S11 and relay K13 regulates the oven temperature at 70° C. When the oven temperature is below 70° C, thermostat S11 is open and relay K13 is de-energized. Line voltage is applied through safety thermostat S12 to heater HR1 through contacts 5-7 and 2-4 of relay K13 in the de-energized condition. When the oven temperature reaches 70° C, thermostat S11 closes. This applies line voltage to rectifiers CR9, CR10, CR11, and CR12 which supply direct current to energize relay K13 and remove power from the heater. The safety thermostat (S12), set to open at 90° C, prevents overheating of the oven in case of failure of the control thermostat S11, the rectifiers or relay K13.

(PART II)

CHAPTER 2

CORRECTIVE MAINTENANCE

Section I. GENERAL TROUBLE-SHOOTING INFORMATION

30. General Instructions

a. Trouble-shooting at higher maintenance levels includes all the techniques outlined for organizational maintenance and any special or additional techniques required to isolate a defective part. The following maintenance procedures are not complete in themselves, but supplement the procedures described in organizational maintenance. The systematic trouble-shooting procedure which begins with the operational and sectionalization checks performed at an organizational level, must be completed by further localizing and isolating techniques.

b. Trouble-shooting may be performed while the equipment is operating as part of a system or, if necessary after the equipment has been removed from service. When trouble occurs, certain observations and substitution of spares can be made which will help in determining whether the local equipment is at fault or if the trouble exists elsewhere in the system. Usually, when trouble-shooting is performed while the equipment is operating as part of a system, it is done at the organizational level. Some trouble-shooting at a higher level can be done with the synchronizer removed from its associated equipment, however, a 160 ms teletype signal is necessary to completely check out the receive functions. The correct signal can be provided by another synchronizer, TSEC/KW-9 combination. A TSEC/KW-9 must be available for a complete checkout of the output functions of the synchronizer. The following paragraphs describe the systematic procedures to be followed which will enable the repairman to isolate the cause of the trouble and correct the fault.

31. Trouble-Shooting Procedures

a. General. The first step in servicing a defective piece of equipment is to sectionalize the fault. Sectionalization means tracing the fault to the major component (such as a plug-in logic card). Refer to Part I of the instruction manual for sectionalization procedures. The second step is to localize the fault. Localization means tracing the fault to the defective stage. The third step, isolation, means tracing the fault to the defective part.

Some faults, such as burned out resistors, arcing or shorted transformers, can often be isolated by sight, smell, or hearing. The majority of faults, however, must be isolated by checking voltages, resistances, and waveforms.

b. Sectionalization. If the trouble has not been sectionalized, follow the procedures and trouble-shooting check list for organizational maintenance to trace the trouble to the faulty card, the power supply, or the relay circuitry.

c. Localization. Procedures are outlined in the trouble-shooting charts (par. 35), for localizing troubles to the individual circuit or stage of a subassembly.

d. Isolation. When trouble has been localized to a particular stage use the techniques and information in paragraph 36 to isolate the defective part.

32. Tools and Test Equipment Required

The tools and test equipment required for maintenance above the organizational level are listed below.

a. Tool Equipment TE-50B.

b. Multimeter AN/URM-105

c. Vacuum tube voltmeter.

d. Oscilloscope, TEKTRONIX 535 or equivalent, with dual trace preamplifier.

33. Auxiliary Equipment Required for Bench Testing

a. Bench Trouble-Shooting. The following auxiliary equipment is necessary for trouble-shooting of a synchronizer.

(1) An additional Synchronizer, Electrical, SN-228(XC-2)/G.

(2) TSEC/KW-9 and associated components.

(3) Teletypewriter TT-98B/FG.

(4) Teletypewriter Reperforator TT-76A/GGC.

(5) Bench test assembly (not furnished). This assembly is used to connect two synchronizer systems by TTY relays to simulate a half-duplex radio link, and is detailed in c. below.

b. Final Bench Testing. The following additional equipment is necessary for a complete bench test of the repaired equipment in simulation of half-duplex operation.

(1) An additional TSEC/KW-9 and associated components.

(2) Teletypewriter TT-98B/FG.

(3) Teletypewriter Reperforator TT-76A/GGC.

c. Bench Test Assembly. The diagram in figure 28 shows a suitable bench test assembly. Substitutions for the specific components indicated may be used as long as the following operating conditions are met:

(1) Relay winding 1-8 (relay A) and loop resistor R1 simulating a transmitter/modulator input at station A.

(2) Relay contacts 5-6 (in relay B) simulating a receiver/converter output at station A.

(3) Relay winding 1-8 (relay B) and loop resistor R2 simulating a transmitter/modulator input at station B.

(4) Relay contacts 5-6 (relay A) simulating a receiver/converter output at station B.

d. Power Supply. A 12 volt power supply is necessary to furnish bias coil (windings 2-3) current for the TTY relays used in the bench test assembly.

Section II. TROUBLE-SHOOTING AND REPAIRS

34. Localizing Troubles

The trouble-shooting charts are designed to supplement the equipment performance check list, and the trouble-shooting check list in Part I of this manual. The trouble-shooting charts list tests and resulting symptoms of improper operation. The probable trouble and the procedure for isolating the faulty component are also listed.

a. Use of Charts. The charts are made on the assumption that the trouble has been sectionalized to the card or subassembly given in the chart title, and that the remainder of the synchronizer is operating properly. The pin numbers called out in the charts can be found in the schematic and wiring diagrams. Waveform diagrams pertinent to the card or circuit are those seen with the synchronizer set for 60 wpm operation.

b. Use of Oscilloscope. The waveform diagrams represent the correct timing and amplitude information as presented on an oscilloscope. The mode of oscilloscope triggering is indicated (external or internal) as well as the polarity. After the oscilloscope probe has been connected, if an incorrect indication has been observed at the collector of any flip-flop, reset the circuitry before assuming that a fault exists. Resetting is accomplished by operating the synchronizer AC POWER switch to OFF momentarily and then returning it to ON. Always use high impedance probes and shielded leads on the oscilloscope. If the synchronizer is being tested in the START mode, the START-STOP switch must be operated to STOP momentarily and then back to START after each reset cycle.

c. Use of the Extender Card. An extender card is supplied to be introduced between a logic card and the interconnecting board. This raises the connector pins of the card above the rails of the other cards for easy access.

d. Set-up of Synchronizer Prior to Using Trouble-Shooting Chart.

(1) Unless otherwise specified, the synchronizer switches should be set as follows:

Switch	Position
DELAY CORRECTOR - OFF	OFF
CHECK-NORMAL	NORMAL
STOP-START	STOP
P-C	C
SEND-MARK HOLD-RECEIVE	RECEIVE
AC POWER	ON

(2) When a 160 ms TTY signal is required in the trouble-shooting tests, a sending synchronizer and

TSEC/KW-9 combination must be connected through the bench test assembly (par. 33c.) as shown in figure 28. For detailed information on connecting the TSEC/KW-9 and teletypewriters to the synchronizer, refer to the installation procedures for the AN/GRC-46 in Part I of this manual. The bench test assembly connections are used in place of the XMTR/MOD and REC/CONV connections. Detailed operating instructions for the synchronizer and the TSEC/KW-9 are given in KAO-86A/TSEC and KAO-49A/TSEC respectively.

e. Trouble-Shooting Logic Circuit Interconnecting Board, Relays, and Switches. When trouble has been sectionalized to the main chassis (not corrected by card placement or power supply checks) it must be determined if the trouble exists in the logic card compartment or the input-output relay switching compartment. By using the Test and Sympton column of the trouble-shooting charts (good cards assumed) an incorrect indication will point to a fault in the logic card compartment. The following tests must be made with all of the logic cards removed:

(1) Interconnecting Board. Continuity checks with an

ohmeter should be made from pin to pin wherever a connection is shown on the wiring diagrams (figs. 29 and 30).

(2) Switches. Continuity checks should be made through the closed contacts on all toggle switches shown in the schematic diagrams (figs. 13 and 14), and wiring diagrams (figs. 29 and 32). Check switches operated to all possible positions.

(3) Send-Receive Relays. Continuity checks should be made through the closed contacts on relays K11 and K12 (fig. 13) in both the energized and de-energized conditions. Refer to the resistance chart (par 37b.). The relays may be energized by grounding terminal G of either relay (synchronizer power on). If either relay will not energize, check coil resistance, as indicated in the chart.

f. Trouble-Shooting Input-Output Relay Circuits (figs. 14 and 31)

(1) If a source of trouble has been sectionalized to to the input-output relay circuitry, the possibility of faulty cables should not be overlooked.

Unless cables are available that are known to be good, a continuity check should be made on all cables. A cable connector wiring diagram is shown in figure 33.

(2) The coils and contacts of the wired-in relays can be tested without moving the relays, by following the instructions in the trouble-shooting chart (par. 35). Figures 24 through 27 can be used in conjunction with the trouble-shooting chart in tracing the correct signal path.

35. Trouble-Shooting Charts.

In using these charts, perform the tests of a card sub-assembly in numerical sequence as indicated.

a. Card A (fig. 5 and 16).

	Test and Symptom	Probable Trouble	Procedure
1.	No output at pin A-1 with SEND-MARK HOLD-RE-CEIVE switch at SEND.	a. Ring counter not running. Faulty flip-flop stage FF1 through FF8.	a. Test flip-flop stages FF1 through FF8.
		b. Faulty reset diode CR103.	b. Test diode.
2.	Incorrect timing of the output of FF1 at pin A-1.	a. Faulty diode CR103.	a. Test diode and circuitry.
		b. Faulty diode CR104.	b. Test diode and circuitry.
3.	Incorrect timing of the output of FF2 at pin A-2.	a. Faulty diode CR109.	a. Test diode and circuitry.
		b. Faulty diode CR108.	b. Test diode and circuitry.

a. Card A (fig. 5 and 16) (Con't).

	Test and Symptom	Probable Trouble	Procedure
4.	Incorrect timing of the output of FF3 at pin A-3.	a. Faulty diode CR115. b. Faulty diode CR114.	a. Test diode and circuitry. b. Test diode and circuitry.
5.	Incorrect timing of the output of FF4 at pin A-4.	a. Faulty diode CR121. b. Faulty diode CR120.	a. Test diode and circuitry. b. Test diode and circuitry.
6.	Incorrect timing of the output of FF5 at pin A-5.	a. Faulty diode CR127. b. Faulty diode CR126.	a. Test diode and circuitry. b. Test diode and circuitry.
7.	Incorrect timing of the output of FF6 at pin A-6.	a. Faulty diode CR133.	a. Test diode and circuitry.

a. Card A (fig. 5 and 16) (Con't).

	Test and Symptom	Probably Trouble	Procedure
		b. Faulty diode CR132.	b. Test diode and circuitry.
8.	Incorrect timing of the output of FF7 at pin A-8.	a. Faulty diode CR140.	a. Test diode and circuitry.
		b. Faulty diode CR139.	b. Test diode and circuitry.
9.	Incorrect timing of the output of FF8 at pin A-10.	a. Faulty diode CR145.	a. Test diode and circuitry.
		b. Faulty diode CR144.	b. Test diode and circuitry.
10.	Operate SPECIAL CHARACTER switch momentarily. No 11 volt, 160 ms square wave with 50% duty cycle	Faulty CR136.	Test diode and circuitry.

a. Card A (fig. 5 and 16) (Con't).

	Test and Symptom	Probable Trouble	Procedure
	seen at pin H-12.	Faulty phasing gate in gates G1 through G8.	Refer to item 12.
11.	Provide a continuous 160 ms TTY signal for the receive input to the synchronizer (par. 34d). Operate SEND-MARK HOLD-RECEIVE switch to RECEIVE. Display the output of FF8 pin A-10 on trace "A" and display the phasing gate input signal at pin A-22 on trace "B" of a dual trace oscp. The phasing		

a. Card A (fig. 5 and 16) (Con't).

	Test and Symptom	Probable Trouble	Procedure
	gate input pulse does not occur at the leading edge of FF8 output signal. X marks the correct phasing point.		
12.	The input pulse pin A-22 occurs more than 14 ms to the right of point X.	Faulty fast retard gate in gates G1, G2, or G3.	Test gate circuitry and diodes CR105, CR110, and CR116.
13.	The input pulse pin A-22 occurs less than 14 ms to the right of point X.	Faulty slow retard gate G8.	Test gate circuitry and diode CR146.
14.	The input pulse pin A-22 occurs more than 14 ms	Faulty fast advance gate in	Test gate circuitry and diodes CR122, CR128, CR134.

a. Card A (fig. 5 and 16) (Con't).

	Test and Symptom	Probable Trouble	Procedure
	to the left of point X.	gates G4, G5, G6.	
15.	The input pulse pin A-22 occurs less than 14 ms to the left of point X.	Faulty slow advance gate G7.	Test gate circuitry and diode CR141.
16.	With a test lead momentarily short the oscillator output to chassis (green test jack J1011 on card J rail). The input will disappear for a few seconds and reappear in one of the positions described in items 12,	Faulty phasing gate.	Refer to items 12, 13, 14, and 15, and use the step which applies to the observed symptom.

a. Card A (fig. 5 and 16) (Con't).

	Test and Symptom	Probable Trouble	Procedure
	13, 14, or 15. Within 10 seconds the pulse should return to point X. Repeat the above test until the input pulse (pin A-22) has appeared in each of the four positions described in items 12, 13, 14, and 15. If the input pulse does not return to point X a malfunction is indicated		

b. Card B (fig. 4).

	Test and Symptom	Probable Trouble	Procedure
1.	No output (fig. 21) at pin B-14 with synchronizer in receive mode.	a. Faulty FF9 or gate G10.	a. Check cathode of CR207 for 2 KC pulses. If no output is found test FF9 and gate G10.
		b. Faulty flip-flop (FF10 through FF12).	b. Trace progress of the square wave signal at the collector of Q202, Q206, and Q208.
		c. Faulty FF13 or gate G11.	c. Check cathode of CR224 for 10 volt positive pulses with approximately 4 ms repetition rate. If no output is found make tests on FF13 and gate G11.
		d. Faulty FF15, FF16, or SS1.	d. Trace progress of the square wave signal at the collector of Q214, Q216, and Q218. Make tests on the stage where signal disappears.

c. Card C (fig. 7).

	Test and Symptom	Probable Trouble	Procedure
1.	No output (fig. 18) at pin C-11 with TD signal input to synchronizer SEND-MARK-HOLD-RECEIVE switch at SEND.	a. Ring counter not running. Faulty flip-flop stage (FF 17 through FF22).	a. Make tests in flip-flop stages FF17 through FF22.
		b. Faulty reset diode CR321.	b. Test diode
2.	Seven ms, 11 volt positive pulse does not appear at pin C-14 each time the SEND-MARK-HOLD-RECEIVE switch is operated to SEND or RECEIVE.	a. Faulty SS8.	a. Make tests on SS8.
		b. Faulty diode CR306.	b. Test diode.
3.	Incorrect timing of the	a. Faulty diode	a. Test diode and circuitry.

c. Card C (fig. 7) (Con't).

	Test and Symptom	Probable Trouble	Procedure
	output of FF17 (fig. 18) at pin C-4.	CR303.	
		b. Faulty diode CR304.	b. Test diode and circuitry.
4.	Incorrect timing of the output of FF18 (fig. 18) at pin C-5.	a. Faulty diode CR309.	a. Test diode and circuitry.
		b. Faulty diode CR310.	b. Test diode and circuitry.
5.	Incorrect timing of the output of FF19 (fig. 18) at pin C-8.	a. Faulty diode CR313.	a. Test diode and circuitry.
		b. Faulty diode CR314.	b. Test diode and circuitry.
6.	Incorrect timing of the output of FF20 (fig. 18) at pin C-9.	a. Faulty diode CR317.	a. Test diode and circuitry.
		b. Faulty diode	b. Test diode and circuitry.

c. Card C (fig. 7) (Con't).

	Test and Symptom	Probable Trouble	Procedure
		CR318.	
7.	Incorrect timing of the output of FF21 (fig. 18) at pin C-11.	Faulty diode CR321.	Test diode and circuitry.
8.	Operate SEND-MARK-HOLD-RECEIVE switch to RECEIVE. Receive input on MARK, no output (fig. 21) at pin C-4.	Ring counter not running. Faulty FF22.	Make tests on FF22.
9.	Incorrect timing of the output of FF17 (fig. 21) at pin C-4.	a. Faulty diode CR303. b. Faulty diode CR304.	a. Test diode and circuitry. b. Test diode and circuitry.
10.	Incorrect timing of the	a. Faulty diode	a. Test diode and circuitry.

c. Card C (fig. 7) (Con't).

	Test and Symptom	Probable Trouble	Procedure
	output of FF18 (fig. 21) at pin C-5.	CR309.	
		b. Faulty diode CR310.	b. Test diode and circuitry.
11.	Incorrect timing of the output of FF19 (fig. 21) at pin C-8.	a. Faulty diode CR313	a. Test diode and circuitry.
		b. Faulty diode CR314.	b. Test diode and circuitry.
12.	Incorrect timing of the output of FF20 (fig. 21) at pin C-9.	a. Faulty diode CR317.	a. Test diode and circuitry.
		b. Faulty diode CR318.	b. Test diode and circuitry.
13.	Incorrect timing of the output of FF21 (fig. 21) at pin C-11.	Faulty diode CR321.	Test diode and circuitry.

c. Card C (fig. 7) (Con't).

	Test and Symptom	Probable Trouble	Procedure
14.	Incorrect timing of the output of FF22 at pin C-13.	Faulty diode CR324.	Test diode and circuitry.

d. Card D (fig. 8 and 19).

	Test and Symptom	Probable Trouble	Procedure
1.	Output signals pins D-11 and D-12 not similar to figure 19 with LETTERS and BLANK input signals to synchronizer as specified in the figure. SEND-MARK-HOLD-RECEIVE switch at SEND.	Faulty storage flip-flop or associated gates.	Proceed to item 2.

d. Card D (fig. 8 and 19) (Con't).

	Test and Symptom	Probable Trouble	Procedure
2.	First baud pulse absent at pin D-11 with LETTERS input or present with BLANK input.	a. Faulty gate G38 or gate G13.	a. Make tests on gates G38 and G13.
		b. Faulty FF29.	b. Make tests on FF29.
3.	Second baud pulse absent at pin D-11 with LETTERS input or present with BLANK input.	a. Faulty gate G39 or gate G15.	a. Make tests on gates G39 and G15.
		b. Faulty FF30.	b. Make tests on FF30.
4.	Third baud pulse absent at pin D-11 with LETTERS input or present with Blank input.	a. Faulty gate G40 or gate G17.	a. Make tests on gates G40 and G17.
		b. Faulty FF31.	b. Make tests on FF31.
5.	Fourth baud pulse absent at pin D-11 with LETTERS	a. Faulty gate G41 or gate G19.	a. Make tests on gates G41 and G19.

d. Card D (fig. 8 and 19) (Con't).

	Test and Symptom	Probable Trouble	Procedure
	input or present with BLANK input.	b. Faulty FF32.	b. Make tests on FF32.
6.	Fifth baud pulse absent at pin D-11 with LETTERS input or present with BLANK input.	a. Faulty gate G42 or gate G21. b. Faulty FF33.	a. Make tests on gates G42 and G21. b. Make tests on FF33.
7.	First baud pulse absent at pin D-12 with BLANK input or present with LETTERS input.	a. Faulty gate G38 or gate G14. b. Faulty FF29.	a. Make tests on G38 and G14. b. Make tests on FF29.
8.	Second baud pulse absent at pin D-12 with BLANK input or present with LETTERS input.	a. Faulty gate G39 or gate G16. b. Faulty FF30.	a. Make tests on gates G39 and G16. b. Make tests on FF30.

d. Card D (fig. 8 and 19) (Con't).

	Test and Symptom	Probable Trouble	Procedure
9.	Third baud pulse absent at pin D-12 with BLANK input or present with LETTERS input.	a. Faulty gate G40 or gate G18. b. Faulty FF31.	a. Make tests on gates G40 and G18. b. Make tests on FF31.
10.	Fourth baud pulse absent at pin D-12 with BLANK input or present with LETTERS input.	a. Faulty gate G41 or gate G20. b. Faulty FF32.	a. Make tests on gates G41 and G20. b. Make tests on FF32.
11.	Fifth baud pulse absent at pin D-12 with BLANK input or present with LETTERS input.	a. Faulty gate G42 or gate G22. b. Faulty FF33.	a. Make tests on gates G42 and G22. b. Make test on FF33.
12.	Trigger oscp. (ext.-) from -12volt line (pin	a. Faulty reset driver Q401.	a. Make tests on Q401.

d. Card D (fig. 8 and 19) (Con't).

	Test and Symptom	Probable Trouble	Procedure
	D-15). Operate POWER switch ON and OFF. Voltage at pin D-18 does not remain at zero for approximately 200 ms after the -12 volts (pin D-15) appears.	b. Faulty diode CR412.	b. Check diode CR412.

e. Card E (fig. 10 and 21).

	Test and Symptom	Probable Trouble	Procedure
1.	Provide a continuous 160 ms TTY signal for the receive input to the synchronizer (par. 34d).	Faulty Q501, gate G24, or SS2.	Make tests on Q501, gate G24, and SS2.

e. Card E (fig. 10 and 21) (Con't).

	Test and Symptom	Probable Trouble	Procedure
	Operate SEND-MARK-HOLD-RECEIVE switch to RECEIVE. Display the input TTY signal pin E-3 on trace "A" and display the signal at pin E-5 on trace "B" of a dual trace oscp. No signal at pin E-5.		
2.	Signal at pin E-5 appear consistently other than at the correct time noted in figure 21 (compared to the TTY signal pin E-3)	Faulty gate G24.	Make tests on gate G24.

e. Card E (fig. 10 and 12) (Con't).

	Test and Symptom	Probable Trouble	Procedure
3.	With TTY input as in item 1 a positive 12 v. 20μsec pulse is seen at the collector of Q509.	Faulty SS3 or Q506.	Make tests on SS3 and Q506.
4.	With no TTY signal input to the synchronizer check the output at the collector of Q509. No positive 12 v. 20μsec pulse at the collector of Q509.	Faulty Q509.	Make tests on Q509.
5.	With TTY input as in item 1 observe the signal at the emitter of	Faulty FF40 or Q510.	Make tests on FF40 or Q510.

e. Card E (fig. 10 and 12) (Con't).

	Test and Symptom	Probable Trouble	Procedure
	Q510. No negative 11 v. 11 ms pulse seen at Q510 each character.		
6.	No 11 volt pulse (spike) at pin E-6 a few seconds after TTY input is applied.	a. Faulty FF41, FF42, FF43, or FF44.	a. Trace progress of the 11 volt square wave signal, at the collector of Q512, Q514, and Q516 in turn. If output is observed, check for Q517 conduction (near zero volts).
		b. Faulty gate G27.	b. Make tests on gate G27.

f. Card F (fig. 6).

	Test and Symptom	Probable Trouble	Procedure
1.	No output (fig. 21) at pin F-7.	a. Faulty flip-flop (FF23 through FF28).	a. Trace progress of the 11 volt square wave signal at the collector of Q602, Q604, Q606, Q608, Q610, and Q612. Make tests on the stage at which the signal disappears.
		b. Faulty SS4.	b. Make tests on SS4.
2.	Incorrect timing of distributor stages (card C). Refer to c above for correct timing information.	Faulty diode CR626, CR614, CR610, CR619, CR609, CR615, or CR623.	Make tests on the suspected diodes and associated components.
3.	Improper receive mode (card E) operation of	Faulty reset diode CR603,	Test diodes.

f. Card F (fig. 6) (Con't).

	Test and Symptom	Probable Trouble	Procedure
	extractor traced to card F.	CR605, CR625, CR611, CR618, or CR622.	

g. Card G (fig. 9 and 20).

	Test and Symptom	Probable Trouble	Procedure
1.	Operate SEND-MARK-HOLD-RECEIVE switch to SEND. Send-receive relays do not operate. Voltage at pin G-12 does not change from -24 v. to near zero volts.	Faulty send-receive circuitry.	Proceed to item 2.
2.	Operate the SEND-MARK-	a. Faulty gate	a. Test diodes and circuitry.

g. Card G (fig. 9 and 20) (Con't).

	Test and Symptom	Probable Trouble	Procedure
	HOLD-RECEIVE switch alternately between SEND and RECEIVE. The voltage at the collector of Q715 does not alternate between -11 v. and zero v.	diodes CR714 or CR715. b. Faulty FF39.	b. Test FF39.
3.	Operate the SEND-MARK-HOLD-RECEIVE switch as in item 2. Voltage at pin G-12 does not alternate between -24 v. and near zero volts.	Faulty relay driver amplifiers Q717, Q718, and Q719.	Make voltage measurements on Q717, Q718, and Q719 and compare the results with the voltage chart (par. 37a).
4.	No -11 v., 5 ms pulse at pin G-19 with each RE-	Faulty SS9.	Test SS9.

g. Card G (fig. 9 and 20) (Con't).

	Test and Symptom	Probable Trouble	Procedure
	CEIVE to SEND switchover		
5.	No - 11 v., 5 ms pulse at pin G-18 with each SEND to RECEIVE switchover.	Faulty SS10.	Test SS10.
6.	Operate SEND-MARK-HOLD-RECEIVE switch to SEND. Provide input signal to synchronizer from TTY KBD. Output control relay does not operate. No 11 v. transition at pin G-15.	Faulty output control circuit	Proceed to item 2.
7.	No signal at the collec-	Faulty FF47.	Test FF47.

g. Card G (fig. 9 and 20) (Con't).

	Test and Symptom	Probable Trouble	Procedure
	tor of Q703, FF47.		
8.	No signal at the collector of Q707, FF48, pin G-17.	a. Faulty SS5. b. Faulty FF48.	a. Test SS5. b. Test FF48.
9.	No output at pin G-15. Same waveform as at pin G-17 with reversed polarity.	Faulty Q709 or Q710.	Test Q709 and Q710.
10.	Operate SEND-MARK-HOLD-RECEIVE switch to RECEIVE. Provide 160 ms TTY signal for the receive input to the synchronizer (par. 34d).	Faulty FF46.	Test FF46.

g. Card G. (fig. 9 and 20) (Con't).

	Test and Symptom	Probable Trouble	Procedure
	After a special character cycle has been received for synchronizing purposes provide input characters with a short pause between each one. Output control relay does not operate. No 11 v. transition at pin G-15.		
11.	Baud information at pin H-18 (fig. 22) does not correspond to the baud information in the input signal (pin J-5).	Faulty gate G-30 or G-31.	Test gates G-30 and G-31.

h. Card H (fig. 12).

	Test and Symptom	Probable Trouble	Procedure
1.	Operate SEND-MARK-HOLD-RECEIVE switch to SEND. Operate START-STOP switch to START. Blank 11 v., TTY signal does not appear at pins H-18 and H-21, 8 seconds later.	a. Faulty relay driver Q820 or Q822.	a. Test Q820 and Q822.
		b. Faulty FF51.	b. Test FF51.
		c. Faulty gate G-35, diode CR823 or diode CR825.	c. Test gate G35, and diodes CR823, and CR825.
		d. Faulty START-STOP circuitry.	d. Proceed to item 2.
2.	Operate START-STOP switch to START or STOP. Collector of Q807 does not go to zero volts for 8 seconds and then return	Faulty SS6.	Test SS6.

h. Card H (fig. 12) (Con't).

	Test and Symptom	Probable Trouble	Procedure
	to -11 v.		
3.	Operate START-STOP switch to START or STOP. Collector of Q810 (FF49) does not go to -11 v. for 8 seconds and then return to zero volts.	a. Faulty gate drivers Q811 or Q812. b. Faulty gates G33 or G34. c. Faulty FF49.	a. Test collectors of Q811 and Q812 stages for 11 volt transitions at the beginning and end of the 8 second interval. If no signal is observed check Q811 and Q812. b. Test diodes CR811, CR813, and gate circuitry. c. Test FF49.
4.	Collector of Q818 (FF50) does not go to zero v. 8 seconds after the START-STOP switch is operated to START.	Faulty FF50.	Test FF50.

h. Card H (fig. 12) (Con't).

	Test and Symptom	Probable Trouble	Procedure
5.	Collector of Q818 (FF50) does not go to - 11 v. 8 seconds after the STOP-START switch is operated to STOP.	Faulty FF50.	Test FF50.
6.	Voltage at pin H-12 does not go to - 11 v. for 8 seconds after the STOP-START switch is operated to START or STOP and then return to zero v. (Opposite polarity should appear at pin H-11.)	a. Faulty relay driver Q813, or Q816. b. Faulty FF52. c. Faulty gate G36 or gate G37.	a. Test Q813 and Q816. b. Test FF52. c. Test diodes CR808 and CR815 and related circuitry.
7.	Operate SPECIAL CHARAC-	a. Faulty SS7.	a. Test SS7 and related circuitry.

h. Card H (fig. 12) (Con't).

	Test and Symptom	Probable Trouble	Procedure
	TER switch momentarily. No 160 ms signal approximately 80 ms space and 80 ms of mark at pin H-12 for 12 seconds.	b. Faulty CR803.	b. Test CR803.
8.	No special character (as in item 7) obsered for 12 seconds each time the SEND-MARK-HOLD-RECEIVE switch is operated to SEND.	Faulty CR804.	Test CR804.
9.	Operate the SEND-MARK-HOLD-RECEIVE switch to RECEIVE.TTY blank not	Faulty gate G32.	Test CR814.

h. Card H (fig. 12) (Con't).

	Test and Symptom	Probable Trouble	Procedure
	present at pin H-18 when the START-STOP switch is at START and absent when the START-STOP switch is at STOP. (RCVR/CONV input on steady MARK).		
10.	Operate the START-STOP switch to START. Observe the blank TTY signal at pin H-18. Momentarily operate the ADVANCE-RETARD switch to RETARD. The blank TTY signal is	Faulty FF53 or gates G44 and G45.	Test FF53, gate G44, and gate G45.

h. Card H (fig. 12) (Con't).

	Test and Symptom	Probable Trouble	Procedure
	not removed for one character each time the ADVANCE-RETARD switch is operated to RETARD.		

i. Card I (fig. 11).

	Test and Symptom	Probable Trouble	Procedure
1.	Trigger the oscp. with a blank TTY signal (pin H-18) of the synchronizer being used as a 160 ms signal source. Display this signal on trace "A" of a dual	a. Faulty FF38. b. Faulty gate G12	a. Test FF38. b. Test diode CR921 and gate circuitry.

i. Card I (fig. 11) (Con't).

	Test and Symptom	Probable Trouble	Procedure
	trace oscp. This provide a fixed time to which the character regenerator advance can be compared. Disconnect the RCVR/CONV cable from the rear of the synchronizer being tested. Operate the SEND MARK-HOLD-RECEIVE switch to SEND and the START-STOP switch to START. Display the blank TTY signal at pin H-18 on trace "B" of a dual		

i. Card I (fig. 11) (Con't).

	Test and Symptom	Probable Trouble	Procedure
	trace oscp. Operate the SEND-MARK-HOLD-RECEIVE switch to RECEIVE. The signal on trace "B" does not advance 10 ms (move to the left) with respect to the signal on trace "A".		
2.	Signal on trace "B" advances continuously with respect to trace "A".	Binary divider consisting of FF34, FF35, FF36, and FF37, not running.	Check for positive 8 volt puses at the cathode of CR922. If absent and the collector of Q909 measures near zero volts test diode CR922 G-9. Trace the progress of the 11v. square wave signal at the collector

i. Card I (fig. 11) (Con't).

	Test and Symptom	Probable Trouble	Procedure
			of Q902, Q904, Q906, and Q908, in turn. If the signal disappears, test the suspected stage.
3.	Collector of Q909 remains near zero volts.	Faulty FF38.	Test FF38.
4.	Signal on trace "B" continues to advance.	Shorted diode CR921 (G-12).	Test diode CR921.
5.	Signal on trace "B" does not advance exactly 10ms	Faulty diode CR916, CR912, CR908, or CR902	Test diodes CR916, CR908, CR912, CR902.
6.	With the conditions set up as in item 1, operate the SEND-MARK-HOLD-RECEIVE switch to SEND.	Faulty diode CR917, CR913, CR909, or CR901	Test diodes CR917, CR913, CR909 and CR901.

i. Card I (fig. 11) (Con't).

	Test and Symptom	Probable Trouble	Procedure
	Trace "B" does not advance 150 ms		
7.	Momentarily operate the ADVANCE-RETARD switch to ADVANCE. Trace "B" does not advance 160 ms.	Faulty gate 46.	Test diode CR924, and gate circuitry.

j. Card J (fig. 3 and 17).

	Test and Symptom	Probable Trouble	Procedure
1.	No 2KC pulses at pin J-7	Faulty tuning fork amplifier.	Make tests on stages Q1023 through Q1027.
2.	No 2 KC, 11 v. square wave at pin J-8.	Faulty squaring circuit Q1028 and Q1029.	Make tests on stages Q1028 through Q1029.

j. Card J (fig. 3 and 17) (Con't).

	Test and Symptom	Probable Trouble	Procedure
3.	No output at pin J-12 with TTY input to synchronizer and SEND-MARK HOLD-RECEIVE switch at SEND.	Faulty stage in main signal integrator.	Trace the progress of the teletype signal through Q1001 and Q1013 to find the stage where the signal stops. Make tests on the faulty stage.
4.	No 2KC pulses at pin J-9 present for 120 ms out of 160 ms with TD signal input to the synchronizer.	a. Faulty FF45. b. Faulty gate G23.	a. Make tests on FF45. b. Make tests on gate G23.
5.	No 160 ms, 11 v. square wave at pin J-4 when synchronizer TD and KBD inputs are on MARK (send mode).	Faulty stage in mark integrator circuit Q1016 through Q1021.	a. Check cathode of CR1009 for 160 ms sawtooth waveform. If absent test CR1009, Q1017, and Q1018. b. Check collector of Q1019 for 60 ms

j. Card J (fig. 3 and 17) (Con't).

	Test and Symptom	Probable Trouble	Procedure
			sawtooth with 160 ms repitition rate. c. If no output or incorrect output is observed in procedures a and b above, make tests on the suspected stage.
6.	Indicator lamp does not flash when synchronizer TD and KBD inputs are on MARK (send mode).	Faulty lamp driver Q1022.	Test the Q1022 stage.
7.	With synchronizer input on MARK, operate the SEND-MARK-HOLD-RECEIVE switch to RECEIVE. Out-	Faulty Q1028 stage.	Test the Q1028 stage.

j. Card J (fig. 3 and 17) (Con't).

	Test and Symptom	Probable Trouble	Procedure
	put at pin J-12 does not go to zero v. for approximately 800 ms and then return to -11 volts.		
8.	2KC pulses not present at pin J-9 when the synchronizer is in the receive mode.	Diode CR1015 open.	Check diode CR1015.

k. Power Supply (fig. 15).

	Test and Symptom	Probable Trouble	Procedure
1.	No -24 v. at the terminal of C23.	a. Short circuit in C22. b. Faulty CR3 and	a. Test at C22 for short circuit or low resistance. b. Test CR3 and CR4.

k. Power Supply (fig. 15) (Con't).

	Test and Symptom	Probable Trouble	Procedure
		CR4.	
		c. Faulty T1.	c. Test for 40 v AC between terminals 5 and 7 of T1. Check winding resistances (par. 37b).
2.	No -12 v. at the terminal of C24	a. Short circuit in voltage distribution circuits.	a. Test for short circuits in voltage distribution circuits.
		b. Open resistor R17.	b. Test R17.
		c. Shorted zener diode CR9.	c. Test CR9.
3.	Voltage at C24 greater than 14 volts.	Open zener diode CR9.	Test CR9.

k. Power Supply (fig. 15) (Con't).

	Test and Symptom	Probable Trouble	Procedure
4.	No +6 volts at the terminal of C25.	a. Short circuit in voltage distribution circuits.	a. Test for short circuits in distribution circuits.
		b. Open resistor R18.	b. Test R18.
		c. Shorted zener diode CR10.	c. Test CR10.
		d. Shorted C14.	d. Test C14.
		e. Faulty CR5 and CR6.	e. Test CR5 and CR6.
		f. Faulty T1.	f. Test for 18 v AC between terminals 11 and 13 of T1. Check winding resistances (par. 37b).

k. Power Supply (fig. 15) (Con').

	Test and Symptom	Probable Trouble	Procedure
5.	No +130 volts at the terminal so marked on the terminal strip TB5 in the relay compartment.	a. Short circuit in the voltage distribution circuitry.	a. Test for short circuits.
		b. Shorted C15.	b. Test C15 for short circuit and low resistance.
		c. Open R19.	c. Test R19.
		d. Faulty CR7 and CR8.	d. Test CR7 and CR8.
		e. Faulty T1.	e. Test for 210 v AV between terminals 8 and 10 of T1. Check winding resistances (par. 37b).

1. Input-Output Relay Circuitry (fig. 14).

	Test and Symptom	Probable Trouble	Procedure
1.	TSEC/KW-9 indicates a line break (red and green lights both on when TSEC/KW-9 is switched to C). No loop current is indicated.	a. Faulty synchronizer loop supply. b. Faulty relay K1 K4, coil L5, L6 L10, or L11.	a. Refer to power supply troubleshooting chart (k above). b. Refer to voltage chart (item 1, par. 36g), and resistance chart (par. 37b).
2.	Operate synchronizer P-C switch to P. Synchronizer red light IA off.	Faulty relay K9.	Same as item 1b above.
3.	Teletypewriter runs open or does not print received plain text.	Faulty relay K7 K9, K10, or resistor R14.	Same as item 1b above.
4.	Operate SEND-MARK-HOLD-RECEIVE switch to SEND.	Faulty relay K3 K7, K9, or K10.	Refer to voltage chart (par. 36g, item 2).

1. Input-Output Relay Circuitry (fig. 14) (Con't).

	Test and Symptom	Probable Trouble	Procedure
5.	Teletypewriter runs open Sending KBD operative before PLAIN START button is depressed.	Faulty relay K8	Same as item 4 above.
6.	Depress PLAIN START button and immediately begin using keyboard. Teletypewriter inoperative.	Faulty relay K7 K8, K9, resistor R4, or switch S9.	Same as item 4 above.
7.	Teletypewriter becomes inoperative in less than 10 seconds with continuous KBD operation	a. Faulty relay K3 K8, or coil L17. b. Faulty C10.	a. Same as item 1b above. b. Check capacitor.
8.	Teletypewriter does not become inoperative after	Faulty relay K3	Refer to voltage chart (par. 36g, item 2), and resistance chart

1. Input-Output Relay Circuitry (fig. 14) (Con't).

	Test and Symptom	Probable Trouble	Procedure
	a 10 second pause in operation.		(par. 37b).
9.	Operate P-C switch on TSEC/KW-9 and synchronizer to C. Operate SEND-MARK-HOLD-RECEIVE switch to RECEIVE. Green light I3 on synchronizer does not come on.	a. Faulty P-C switch S4. b. Faulty relay K9	a. Make continuity check on S4. b. Refer to voltage chart (par. 36g, item 3), and resistance chart (par. 37b).
10.	Teletypewriter runs open	Faulty relay K6 K9, resistor R10, coil L14, or L16.	Same as item 9b above.
11.	Operate CHECK-NORMAL	Faulty relay K6	Same as item 9b above.

1. Input-Output Relay Circuitry (fig. 14) (Con't).

	Test and Symptom	Probable Trouble	Procedure
	switch to CHECK. Teletypewriter runs open.	or coil L15.	
12.	Alternately short and open the tip to sleeve of the REC/CONV cable plug. Indicator lamp I2 not on with open plug (space) and blinking with shorted plug (mark).	Faulty relay K3 K4, K9, K10, resistor R14, or coil L9.	Same as item 9b above.
13.	Operate SEND-MARK-HOLD-RECEIVE switch to SEND. Teletypewriter runs open.	Faulty K6 or K9	Refer to voltage chart (par. 36g, item 4) and resistance chart (par. 37b).
14.	Operate START-STOP switch to START. Wait 8 seconds	Faulty relay K4 K10, or coil L3	Same as item 13 above.

1. Input-Output Relay Circuitry (fig. 14) (Con't).

	Test and Symptom	Probable Trouble	Procedure
	until the TSEC/KW-9 begins operating. Operate KBD. No home copy.		
15.	Monitor current through the Bench Test Assembly **XMTR**/MOD relay. No current through relay.	Faulty relay K5 K10, K2, coil L12, L13, L7, or L8.	Same as item 13 above.
16.	No fluctuation of XMTR/ MOD current with input signal from KBD or TD.	Faulty relay K5 or coil L4.	Same as item 13 above.

36. Isolating Trouble Within a Stage or Circuit.

When trouble has been localized to a stage or circuit through use of the trouble-shooting chart, the defective part can be isolated by certain voltage and resistance measurements.

a. Flip-flop Testing. If a faulty flip-flop is indicated proceed as follows:

(1) With synchronizer power on, short the green test jack J1011 (top of card J) to chassis to stop drive pulses.

(2) With an oscilloscope or voltmeter see if one collector is at -11 volts (non-conducting) and the other near ground or less than -.2 volt (conducting).

(3) Using a clip lead, momentarily short the -11 volt collector to ground. The collector should remain near ground and the other collector should have changed to -11 volts. Flip-flop voltage readings are given in paragraph 37a. This tests all but the diode input circuitry. Test input diodes as described in f. below.

(4) If the flip-flop will not stay in each of its

two states after being forced there, make resistance measurements of the transistors as indicated in the chart below with power off. Readings are given with the Multimeter AN/URM-105 on the X100 resistance scale. Since polarity of ohmeter voltage affects the reading observe lead polarity. Another meter that does not use a 1.5 volt battery on the X100 scale will not give the same reading. Readings may vary more than 100 percent without necessarily indicating a faulty transistor. The test will, however, indicate open or shorted transistor junctions. Test leads with sharp points are necessary to punch through epoxy coating.

Points of measurement	Lead polarity	Reading
Collector to emitter	Red lead to collector.	2.4 k
	Reversed	Greater than 10 k
Base to emitter	Red lead to base.	100 ohms
	Reversed	Greater than 20 k

(5) Check capacitors for shorts and check resistors. The reading across resistors may be lower than the resistor value due to parallel circuit paths, but a higher reading indicates an open resistor.

(6) Check for possible breaks in the etched wiring by making ohmmeter continuity checks.

(7) If no obvious fault is found, replace the transistor that will not remain in conduction if forced as given in (3) above.

b. Single-shot Testing. The voltage and resistance readings given in a. above also apply to single-shot circuits. A single-shot, however, normally returns to its one stable condition.

c. Emitter Followers. With an oscilloscope see that the output of an emitter follower is a reproduction of its base input signal. If it is not, a faulty transistor is indicated.

d. Voltage Amplifiers. The voltage amplifier stages in the tunig fork oscillator (card J) may be tested by use of the voltage chart (par. 37a.).

e. Inverters or Pulse Amplifiers. Switching transistors for which specific instructions are not given may be tested by signal tracing, voltage, and resistance measurements. Resistance measurements at the collector and base should be the same as those given in a. above. Voltage measurements on transistors are specified in paragraph 37a. should read as follows:

(1) Collector near -12 volts when the base reads slightly positive.

(2) Collector near zero volts when the base reads -.23 volts.

f. Diode Testing. If a faulty diode or diode gate circuit is indicated proceed as follows:

(1) Most of the diodes may be tested for open or short circuits without removing them from the circuit. Use the AN/URM-105 on the X100 scale. A variation in reading of 100 percent is to be expected in good diodes.

Diode	Red lead to cathode (ohms)	Black lead to cathode (ohms)
1N198 - all	200	Greater than 30 K
1N457 - CR803, CR804, CR805, CR1008, CR1009, CR1010	375	Greater than 30 K

Diode	Red lead to cathode (ohms	Black lead to cathode (ohms)
1N457 - CR1002, CR1003	375	450
1N753 - CR1012	375	500
1N753 - CR716	375	Greater than 30 K
1N429 - CR1014	350	350
NOTE: One lead of the following diodes must be disconnected before measuring:		
1N614 - CR3, CR4	250	Infinity
1N538 - CR5, CR6	250	
1N540 - CR7, CR8	250	
50M12ZR5 - CR9	300	Infinity
3Z6A - CR10	250	Infinity

(2) If diodes in the suspected area read normal then check for shorted capacitors, open resistors, or broken etched circuit lines.

g. Testing of Input-output Relay Circuitry. Isolation of a faulty relay contact may be accomplished by use of the following chart. Localization by use of the trouble-shooting chart (par. 35) should precede the following measurements.

(1) Use the AN/URM-105 on the 1000 volt scale and connect the red lead to the first contact of each relay pair in the following chart. A faulty relay contact is indicated by a reading of full loop voltage (approx. 130 volts) where zero is listed as normal.

Test conditions	Points of measurement	Reading (volts)
1. Plain receive. Connect tip to sleeve on the REC/CONV cable plug.	K1 - 4 to 6	0
	K4 - 5 to 4	0
	3 to A	0
	K7 - 3 to 5	0
	2 to A	0
	K9 - A to 1	0
	5 to C	0
	K9 - B to 3	0
	8 to D	0
	K10 - 10 to E	0
2. Plain send. PLAIN-START button not depressed.	K3 - 4 to 6	130
	3 to 2	1.5
	K8 - 1 to 8	0

Test Conditions	Points of measurement	Reading (volts)
a. Insert an open plug into either KBD or TD jack.	a. K8 - 2 to 3	0
b. Depress PLAIN-START button mementarily an release.	b. K3 - 4 to 6	0
	K7 - 8 to D	0
	K8 - 6 to 5	0
c. Depress PLAIN-START button and hold.	c. K8 - 1 to 8	125
	K9 - F to 12	0
	R4	5
d. Remove WHT-GY wire from terminal 3 of relay K8. Remove open plug from KBD or TD jack. (Replace WHT-GY wire after measurement.)	d. K7 - 4 to 5	0
	2 to B	0
	K9 - 5 to C	0
	B to 3	0
	K10 - D to 8	0
	1 to A	0
	K10 - B to 3	0
	5 to C	0
3. Cipher receive. Connect tip to sleeve on the REC/CONV cable plug.	K3 - 3 to 2	1.5
	6 to 7	0, 2 v if faulty

Test conditions	Points of measurement	Reading (volts)
	K4 - D to 9	0, 2 v if faulty
	11 to E	0
	K6 - 3 to 4	0
	2 to 4 (CHECK-NORMAL switch at CHECK.)	0
	K9 - 6 to C	0
	B to 4	0
	A to 2	0
	K10 - 9 to E	0
4. Cipher send.	K4 - 12 to F	0, 12 v if faulty
	8 to 9	0, 2 v if faulty
	10 to E (C4 shorted to chassis)	0, 12 v if faulty

Test Conditions	Points of measurement	Reading (volts)
	K5 - 4 to 3	0
	4 to 2 (C4 shorted to chassis)	0
	K6 - 2 to 4	0
	K9 - 6 to C	0
	B to 4	0
	K10 - A to 2	0, 2 v if faulty
	4 to B	0, 2 v if faulty
	D to 7	0
	6 to C	0

(2) Refer to resistance chart (par. 37b.) for normal relay coil resistance readings.

37. Voltage and Resistance Charts

a. Voltage Chart. The voltages are measured to ground with a voltmeter. When two voltages are given for a single point of measurement, the first reading should be obtained with the synchronizer input on MARK. The second reading should be obtained with the input open or SPACE. A variation in readings of 20 percent is normal.

Item	Component	Collector voltage	Base voltage	Emitter voltage
1.	Flip-flop of single-shot stage:			
	a. conducting transistor	-0.08	-0.23	0
	b. non-conducting transistor	-11.1	-2.6	0
2.	Q1001	-11.5	0	-2
		-2.5	-2.6	-2.4
3.	Q1006	-12	-5	-4.8
4.	Q1009	-11.8	-2.6	-5.6
		-5.5	-5.6	-5.4
5.	Q1010	-12	-11.8	-11.6
		-12	-5.5	-5.4
6.	Q1019	-7.6	-0.9	-0.8
7.	Q1023	-6	-3	-2.9
8.	Q1024	-3.3	-1.5	-1.4

Item	Component	Collector voltage	Base voltage	Emitter voltage
9.	Q1025	-4.5	-3.3	-3.2
10.	Q1026	-6	-4.5	-4.4
11.	Q1027	-9	-2.6	-2.4

b. Resistance Chart. The dc resistance of the relay coils, transformers, and choke coils are listed below:

Item	Component	Conditions for measurement	Terminals	Ohms
1.	K1, K2, or K3 coil		1 to 8	25
			2 to 3	25
2.	K4 coil	Remove WHT wire from terminal 13 of K4	1 to 13	240
3.	K5 coil		1 to 8	240
4.	K6 coil	Remove GRN wire from terminal 8 of K6	1 to 8	240
5.	K7 coil	SEND-MARK HOLD-RECEIVE switch at RECEIVE	1 to 10	350

(PART II)

Item	Component	Conditions for measurement	Terminals	Ohms
6.	K8 coil	Remove WHT-RED wire from terminal 1 of K8 and remove V10 wire from R2 or R3	1 to 8	13 K
7.	K9, K10 coils paralleled	P-C switch at P	G to 13	120
8.	K11, K12 coils paralleled	Remove wire from capacitor C3	G to 13	120
9.	K11, K12 contacts	Energized	D to 7	0
		Energized	F to 11	0
		Energized	A to 2	0
		Energized	B to 4	0
		Energized	E to 9	0
		Energized	C to 6	0
		De-energized	D to 8	0
		De-energized	F to 12	0
		De-energized	A to 1	0
		De-energized	B to 3	0

Item	Component	Conditions for measurement	Terminals	Ohms
		De-energized	E to 10	0
		De-energized	C to 5	0
10.	T1 Primary		1 to 3	1.3
	40 v winding		5 to 7	.4
	18 v winding		11 to 13	6
	210 v winding		8 to 10	30
11.	T2 Primary		4 to 6	45
	Secondary		1 to 3	350
12.	L9, L1001 coil			40
13.	L1, L2, L5, L6, L7, or L8 coil			30
14.	L3, L4, L10, L11, L12, L13, L14, L15, L16, or L17 coil			10

38. Adjusting Tuning Fork Oscillator Frequency

The tuning fork oscillator frequency normally does not require adjustment unless major repair is done on the tuning fork oscillator and/or it is found that a synchronizer will not maintain synchronism for the required length of time.

One of two methods may be used to measure and adjust the oscillator frequency depending upon available equipment.

a. Using a Frequency Counter. If a frequency counter that has a counting time of at least 1000 seconds is available, it may be used to set the fork oscillator frequency. The counter used should be accurate to better than one part per million. Assuming a 1000 second count, the 2000 cps fork oscillator could be set within plus or minus 1.5 parts per million. The 3260 cps fork oscillator could be set within plus or minus 1.3 parts per million. For example, if a 2000 cps oscillator output is counted for 1000 seconds the total count (if exactly tuned) would be 2 million. If the counter registers 2 million and one and the accuracy of the counter is known to be at least 1 part per million, the fork oscillator frequency could be off no more than 1.5 parts per million. The oscillator frequency is adjusted as follows:

(1) Connect the tuning fork oscillator output (green test jack J1011 on rail of card J) to the frequency counted input. The amplitude is approximately 12 volts peak to peak.

(2) Start the counter. At the end of a 1000 second count the reading should be 2 million for the

2000 cps fork and 3.26 million for the 3260 cps fork. Repeat several times to see if results are consistant.

(3) If the 2000 cps count is high, turn potentiometer R1089 (on card J) slightly clockwise. If the count is low, turn potentiometer slightly counter-clockwise. Potentiometer R1088 should be turned if the 3260 cps frequency is being adjusted. One turn of the potentiometer will change the frequency approximately one part per million.

(4) Repeat the 1000 second counting and adjusting procedure until a count within plus or minus one is achieved.

b. Using Another Synchronizer. When another synchronizer that is known to be operating properly is available, it may be used as a reference in adjusting the frequency of a repaired tuning fork oscillator. Proceed as follows:

(1) Externally trigger an oscilloscope with the tuning fork output (green test jack J1011 on the rail of card J) of the reference synchronizer. Display this signal on one trace of a dual trace oscilloscope. Set sweep speed to 100 microsec-

onds per centimeter.

(2) Display the tuning fork output of the repaired synchronizer on the other trace. A certain amount of rapid jitter is normal.

(3) Observe the relative phase of the two square wave signals for several minutes. If the repaired oscillator 2000 cps output drifts to the left the frequency is too high. Turn potentiometer R1089 (on card J) slightly clockwise and again observe drift. Potentiometer R1088 should be turned if the 3260 cps frequency is being adjusted. If the drift is to the right the frequency is low and the potentiometer should be turned slightly counter-clockwise. The observation and adjustment procedure should be repeated until zero or a minimum of drift is achieved.

39. Parts Replacement Techniques

Replacement of parts other than those on the etched circuit cards may be accomplished following the normal techniques used on wired equipment. When replacing parts on the etched circuit cards, certain precautions should be observed so as not to damage the etched wiring or components.

a. Use a pencil type soldering iron with a 25-watt capacity, if available.

b. When removing parts, cut the leads close to the component being removed (if possible) and straighten the lead ends protruding from the board. Heat the solder joint and gently push the lead end through the card from the component side. Extreme care must be used in this operation or the copper conductor will be stripped from the board.

c. When replacing parts, make sure the holes in the board are free of solder before trying to force the new lead through.

d. When soldering transistor and diode leads, solder quickly. Use a heat sink (such as long nose pliers) between the soldered joint and diode.

40. Final Bench Testing

a. Additional Equipment Required. The equipment required for final bench testing is the same as that listed for trouble-shooting (par. 33).

b. Test Setup. Complete bench testing can be done with two synchronizers (one repaired and another auxiliary unit) and their auxiliary equipment connected as a half-duplex network. The bench test assembly (par. 33c.) is used to connect the two systems in place of a radio link. Connection of the TSEC/KW-9 and teletypewriters is detailed in Part I of this manual.

c. Test Procedure. Perform the tests in numerical sequence and look for the correct indication.

Item	Action or Condition	Correct Indication
1.	Set switches as follows: DELAY CORRECTOR - OFF CHECK-NORMAL - NORMAL STOP-START - STOP SEND-MARK HOLD-RECEIVE - RECEIVE P-C - P TSEC/KW-9 P-C - P AC POWER (all equipment) - ON	Teletypewriters may or may not run open because bench test setup has no mark hold feature.
2.	Operate repaired synchronizer SEND-MARK HOLD-RECEIVE switch to SEND. Send test	Receiving teletypewriter ceases to run open but does

Item	Action or Condition	Correct Indication
	message from KBD.	receive text.
3.	Push PLAIN-START button and send test message from KBD.	Receiving teletypewriter does not print test message.
4.	Pause ten seconds and then resume test message.	Receiving teletypewriter does not print text.
5.	Operate SEND-MARK HOLD-RECEIVE switch to RECEIVE.	Teletypewriters may or may not run open.
6.	Operate auxiliary synchronizer SEND-MARK HOLD-RECEIVE switch to SEND. Depress PLAIN-START button and send test message from KBD.	Receiving teletypewriter prints test message.
7.	Operate auxiliary synchronizer SEND-MARK HOLD-RECEIVE switch to RECEIVE.	Teletypewriters may or may not run open.
8.	Refer to KAO-49A/TSEC for TSEC/KW-9 operation. Switch both synchronizers	Teletypewriters cease running open. Green lights go on.

Item	Action or Condition	Correct Indication
	and TSEC/KW-9's to C.	
9.	Operate SEND-MARK HOLD-RECEIVE switch on the repaired synchronizer to SEND.	Special character will be transmitted for 12 seconds. This can be seen by monitoring the current in the bench test assembly sending relay coil. The indicator lamp I2 on the receiving synchronizer will be on during this 12 seconds.
10.	Operate the repaired synchronizer STOP-START switch to START. Within eight seconds operate the receiving synchronizer STOP-START switch to START.	The receiving synchronizer indicator lamp should change from blinking to steady on. At the end of eight seconds, both TSEC/KW-9's should

Item	Action or Condition	Correct Indication
		begin operation. Receiving teletypewriters receive nothing.
11.	Send test messages from KBD and TD.	Home copy teletypewriter prints correct test. Receiving teletypewriter prints correct text. Look for absence of garble between characters and during the speed differential blank when using TD test message.
12.	Stop TD. Operate the repaired synchronizer STOP-START switch to STOP. Within eight seconds operate the receiving synchronizer STOP-START switch to STOP.	The receiving synchronizer indicator lamp should change from blinking to steady on. At the end of eight seconds, both TSEC/KW-9's should

Item	Action or Condition	Correct Indication
		cease operation. The TSEC/KW-9 counters should read the same.
13.	Operate repaired synchronizer SEND-MARK HOLD-RECEIVE switch to RECEIVE. Operate auxiliary synchronizer SEND-MARK HOLD-RECEIVE switch to SEND.	Special character is transmitted for 12 seconds. During this time the receiving synchronizer indicator lamp is on.
14.	Operate the auxiliary synchronizer STOP-START switch to START. Within eight seconds operate the receiving synchronizer STOP-START switch to START.	The receiving synchronizer indicator lamp should change from blinking to steady on. At the end of eight seconds, both TSEC/KW-9's should begin operation. Receiving teletypewriters should receive nothing.

Item	Action or Condition	Correct Indication
15.	Send test messages from KBD or TD.	Receiving teletypewriter prints correct text. Look for absence of garble between characters.
16.	Operate repaired synchronizer ADVANCE-RETARD switch to RETARD.	Receiving teletypewriter prints garble.
17.	Operate repaired synchronizer ADVANCE-RETARD switch to ADVANCE.	Receiving teletypewriter should begin printing text within three seconds.
18.	Stop TD. Operate auxiliary synchronizer STOP-START switch to STOP. Within eight seconds operate receiving synchronizer STOP-START switch to STOP.	At the end of eight seconds both TSEC/KW-9's should cease operation with their counters reading the same.

(PART II)

APPENDIX

REFERENCES

Following is a list of applicable references available to maintenance personnel of Synchronizer, Electrical, SN-228(XC-2)/G.

TM 11-264B	Radio Set AN/GRC-26D
TM 11-690	Basic Theory and Application of Transistors.
TM 11-2225	Teletypewriter Sets AN/GGC-3 and AN/GGC-3A, and Teletypewriter Reperforator Transmitters TT-76/GGC, TT-76A/GGC and TT-76B/GGC.
TM 11-5815-200-35	Field and Depot Maintenance, Teletypewriter Sets AN/GGC-20, AN/FGC-21, AN/UGC-4, and Teleprinter TT-259/FG.
TM 11-5815-204-35	Field and Depot Maintenance, Radio Teletypewriter Sets AN/GRC-46 and AN/VRC-29.

(PART II)

KAO-86A/TSEC	Operating Instructions for Electrical Synchronizer, SN-228(XC-2)/G.
KAM-10/TSEC	Repair and Maintenance Instructions for TSEC/KW-9.
TB SIG 340	Cipher Machine TSEC/KW-9.

Instruction Manual for Synchronizer, Electrical, SN-228(XC-2)/G, Part I, Installation and Organizational Maintenance.

(PART II)

GLOSSARY

Section I. ABBREVIATIONS

cps	cycles per second
wpm	words per minute
TTY	teletype
ac	alternating current
ma	milliamperes
TD	transmitter-distributor
KBD	keyboard
dc	direct current
oscp	oscilloscope
VTVM	vacuum tube voltmeter

Section II. DEFINITIONS

Flip-flop. A bistable multivibrator having two stable states and two input terminals each of which corresponds with one of the two states.

Single-shot. A monostable multivibrator with only one stable state of operation. A suitable trigger pulse will cause it to pass into a semistable state where it remains for a given time before returning to its original stable state.

AND gate. A circuit which permits two or more pulse circuits to be connected together to a common load and whose output is energized only when every input pulse is applied simultaneously.

OR gate. A circuit that permits two or more pulse circuits to be connected together to a common load and whose output is energized when a pulse is applied to any one or more of the inputs.

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Block diagram, simplified	3	77
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Distributor	10,14	89,94
Extensor	11	91

	Paragraph	Page
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Main signal integrator	8	84
Mark integrator	25	110
Miscellaneous circuitry	27	113
Output control	12,18,20	93,102 104
Phasing	15,16	95,98
Power supply	29	123
Received signal readout	17	101
Schematic diagram	4	79
Send-receive switching	10	103
Special character	23	107
Start-stop	24,26	108,112
Transmission delay correction	20	104
Tuning fork oscillator	5	80
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Tools and test equipment	32	128
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Trouble-shooting:		
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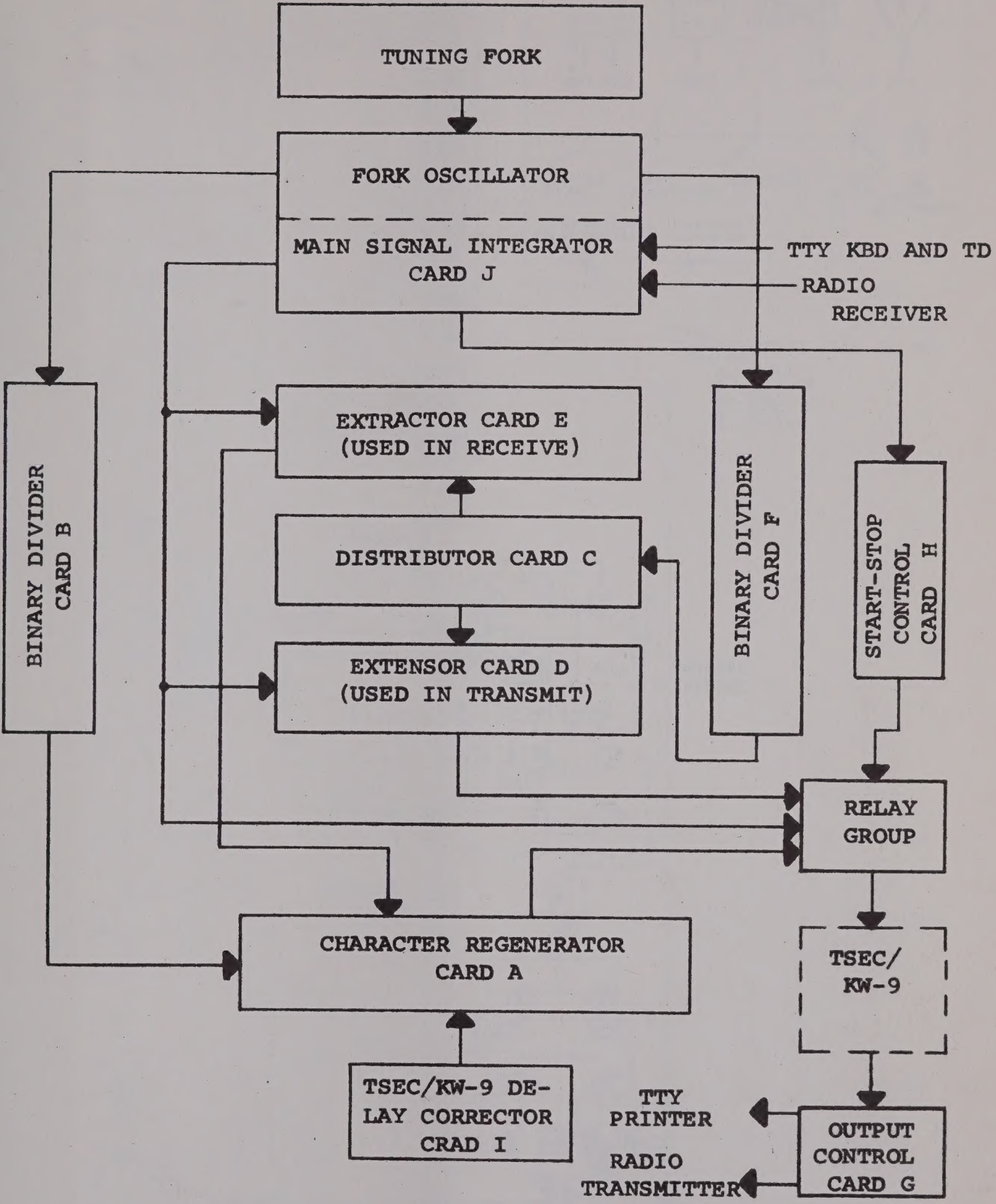

TUNING FORK
FORK OSCILLATOR
MAIN SIGNAL INTEGRATOR CARD J
TTY KBD AND TD
RADIO RECEIVER
BINARY DIVIDER CARD B
EXTRACTOR CARD E (USED IN RECEIVE)
DISTRIBUTOR CARD C
EXTENSOR CARD D (USED IN TRANSMIT)
BINARY DIVIDER CARD F
START-STOP CONTROL CARD H
RELAY GROUP
CHARACTER REGENERATOR CARD A
TSEC/ KW-9
TSEC/KW-9 DELAY CORRECTOR CRAD I
TTY PRINTER
RADIO TRANSMITTER
OUTPUT CONTROL CARD G

FIG. 1. SN-228(XC-2)/G, SIMPLIFIED BLOCK DIAGRAM.

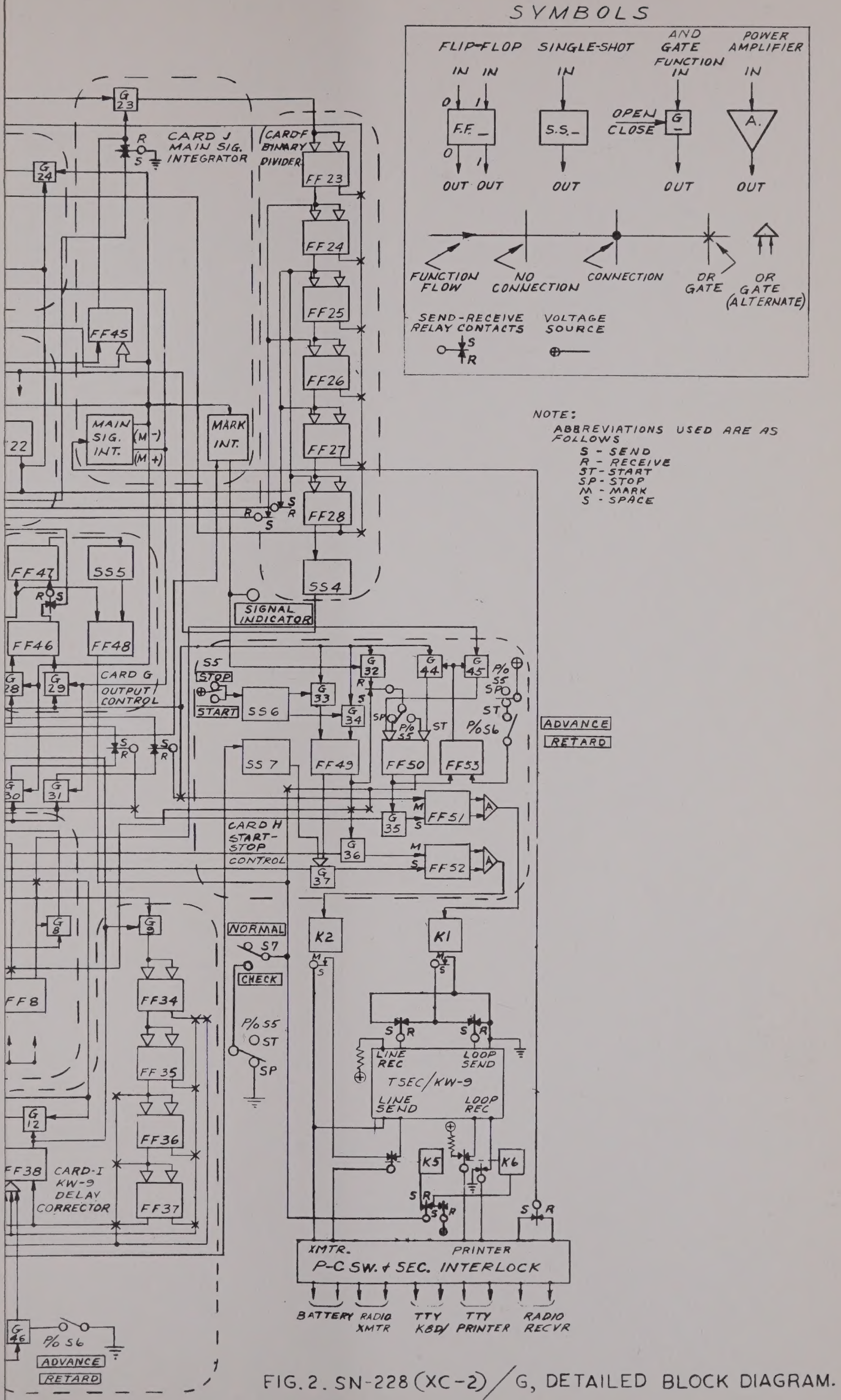

SYMBOLS
FLIP-FLOP
IN IN
0 1
F.F. _
0 1
OUT OUT
SINGLE-SHOT
IN
S.S._
OUT
AND GATE FUNCTION
IN
OPEN
CLOSE
G
OUT
POWER AMPLIFIER
IN
A.
OUT
FUNCTION FLOW
NO CONNECTION
CONNECTION
OR GATE
OR GATE (ALTERNATE)
SEND-RECEIVE RELAY CONTACTS
S
R
VOLTAGE SOURCE
NOTE:
ABBREVIATIONS USED ARE AS FOLLOWS
S - SEND
R - RECEIVE
ST - START
SP - STOP
M - MARK
S - SPACE
G 23
G 24
R
S
CARD J MAIN SIG. INTEGRATOR
CARD F BINARY DIVIDER
FF 23
FF 24
FF 25
FF 26
FF 27
FF 28
SS 4
FF45
22
MAIN SIG. INT.
(M-)
(M+)
MARK INT.
SIGNAL INDICATOR
FF47
SS5
FF46
FF48
G 28
G 29
CARD G OUTPUT CONTROL
G 30
G 31
S5
STOP
START
SS6
G 32
G 33
G 34
G 44
G 45
P/o S5
SP
ST
P/o S6
ADVANCE
RETARD
SS 7
FF49
FF50
FF53
FF51
FF52
M
S
A
G 35
G 36
G 37
CARD H START-STOP CONTROL
G 8
G 9
FF8
FF34
FF 35
FF36
FF37
G 12
FF38
CARD-I KW-9 DELAY CORRECTOR
NORMAL
S7
CHECK
P/o S5
ST
SP
K2
K1
LINE REC
LOOP SEND
TSEC/KW-9
LINE SEND
LOOP REC
K5
K6
XMTR.
PRINTER
P-C SW. + SEC. INTERLOCK
BATTERY
RADIO XMTR
TTY KBD/
TTY PRINTER
RADIO RECVR
G 46
P/o S6
ADVANCE
RETARD

FIG. 2. SN-228 (XC-2)/G, DETAILED BLOCK DIAGRAM.

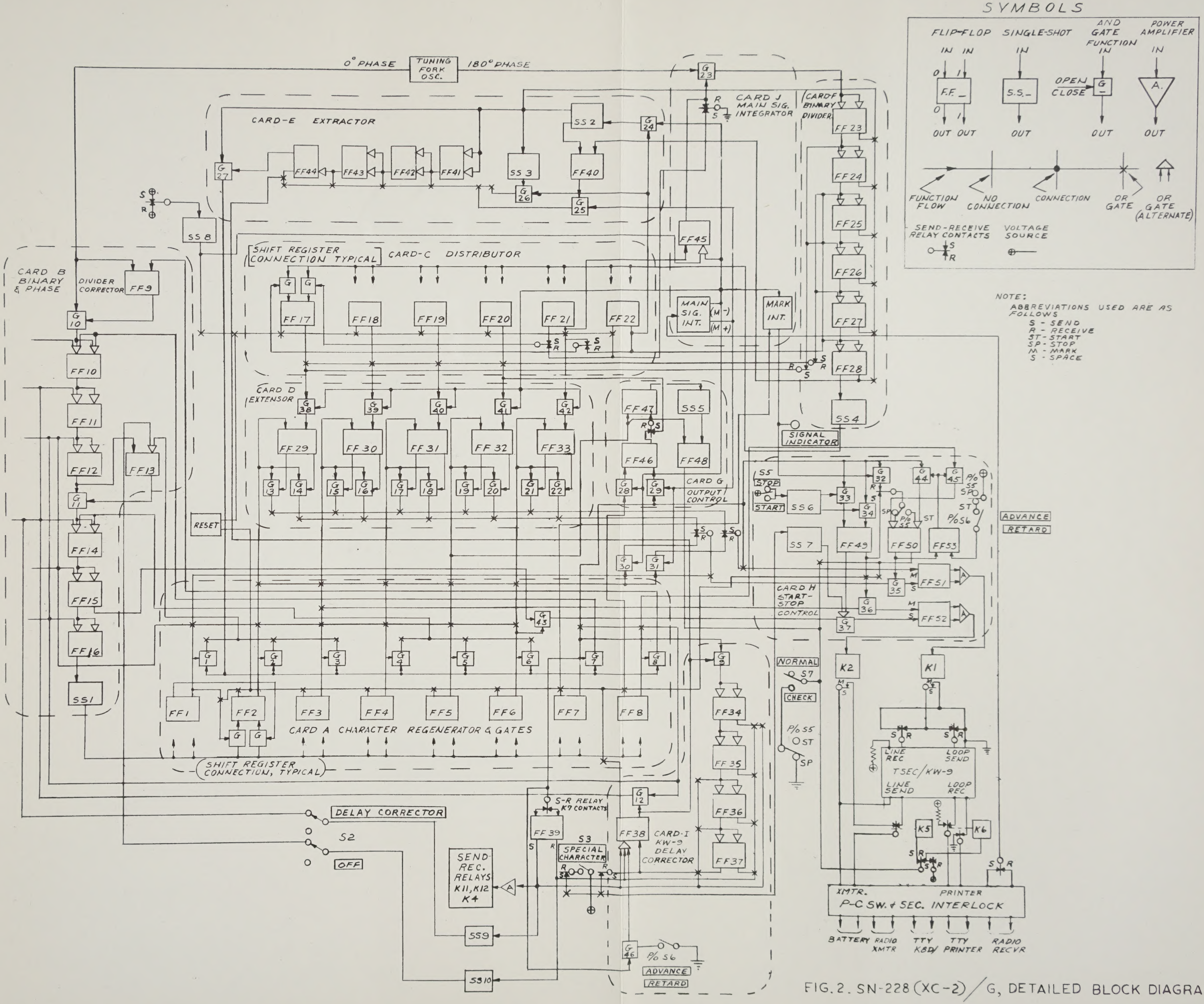
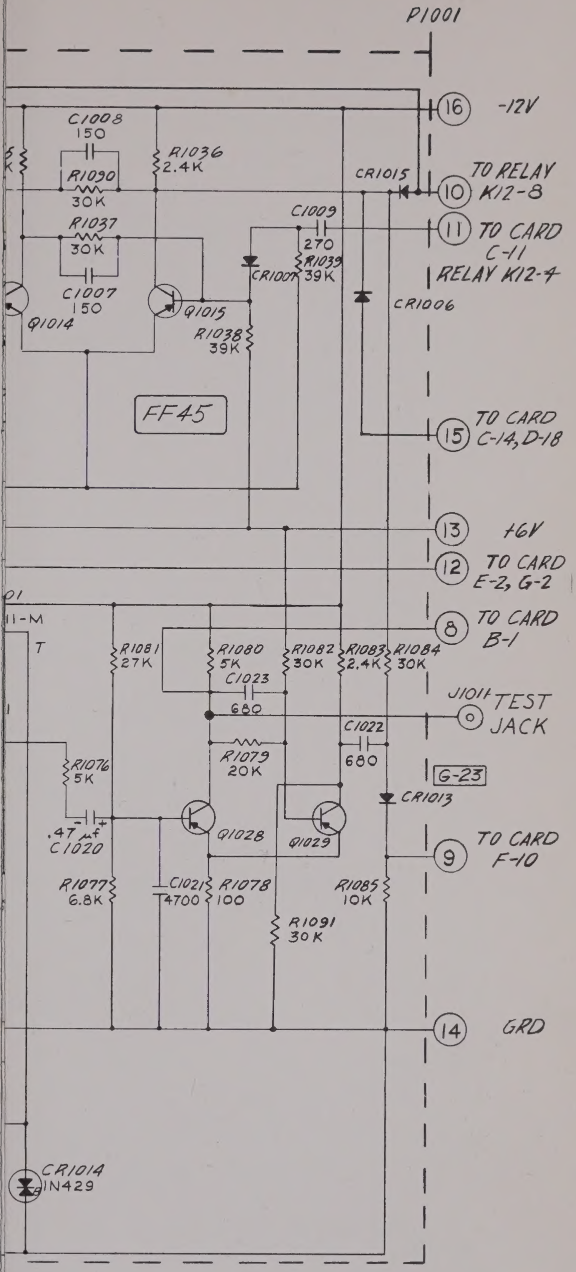
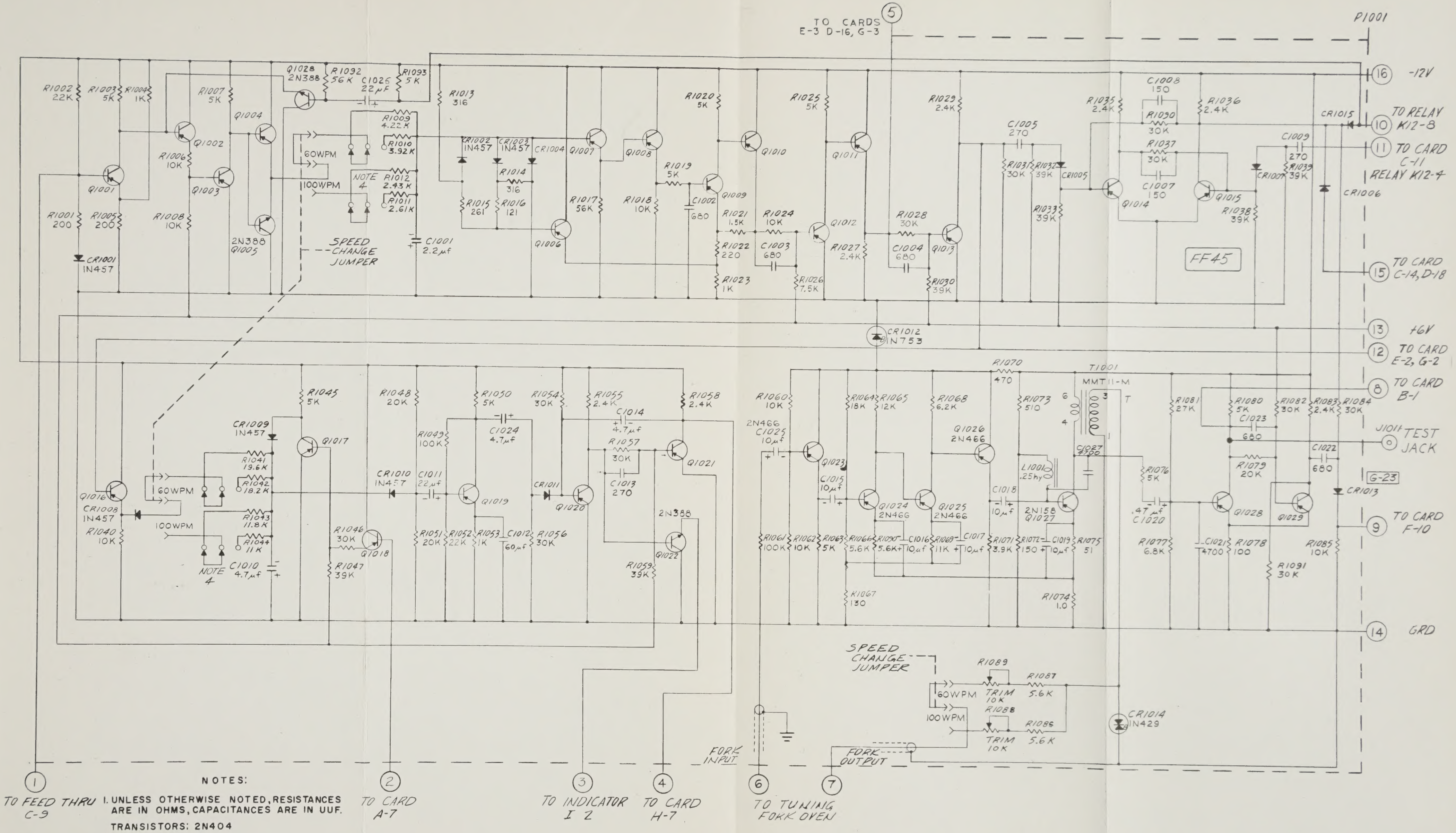

SYMBOLS
FLIP-FLOP
SINGLE-SHOT
AND GATE FUNCTION
POWER AMPLIFIER
IN
0
1
F.F._
S.S._
OPEN
CLOSE
G
A.
OUT
FUNCTION FLOW
NO CONNECTION
CONNECTION
OR GATE
OR GATE (ALTERNATE)
SEND-RECEIVE RELAY CONTACTS
VOLTAGE SOURCE
S
R
NOTE:
ABBREVIATIONS USED ARE AS FOLLOWS
S - SEND
R - RECEIVE
ST - START
SP - STOP
M - MARK
S - SPACE
0° PHASE
TUNING FORK OSC.
180° PHASE
CARD-E EXTRACTOR
FF44
FF43
FF42
FF41
SS 2
SS 3
FF40
G 24
G 26
G 25
G 27
SS 8
G 23
CARD J MAIN SIG. INTEGRATOR
CARD F BINARY DIVIDER
FF 23
FF 24
FF 25
FF 26
FF 27
FF 28
SS 4
FF45
SIGNAL INDICATOR
CARD B BINARY & PHASE
DIVIDER CORRECTOR
FF9
G 10
FF10
FF11
FF12
FF13
G 11
FF14
FF15
FF16
SS1
SHIFT REGISTER CONNECTION TYPICAL
CARD-C DISTRIBUTOR
FF 17
FF18
FF19
FF20
FF 21
FF22
MAIN SIG. INT.
(M-)
(M+)
MARK INT.
CARD D EXTENSOR
G 38
G 39
G 40
G 41
G 42
FF 29
FF 30
FF 31
FF 32
FF33
G 13
G 14
G 15
G 16
G 17
G 18
G 19
G 20
G 21
G 22
FF 47
SS5
FF46
FF48
G 28
G 29
CARD G OUTPUT CONTROL
RESET
G 30
G 31
SS STOP
START
SS 6
SS 7
G 32
G 33
G 34
G 44
G 45
P/o S5
SP
ST
P/o S6
ADVANCE
RETARD
FF49
FF50
FF53
FF51
FF52
G 35
G 36
G 37
CARD H START-STOP CONTROL
G 43
G 1
G 2
G 3
G 4
G 5
G 6
G 7
G 8
G 9
FF1
FF2
FF3
FF4
FF5
FF6
FF7
FF8
CARD A CHARACTER REGENERATOR & GATES
SHIFT REGISTER CONNECTION, TYPICAL
FF34
FF 35
FF36
FF37
NORMAL
S7
CHECK
P/o S5
ST
SP
K2
K1
M
LINE REC
LOOP SEND
TSEC/KW-9
LINE SEND
LOOP REC
K5
K6
XMTR.
PRINTER
P-C SW. & SEC. INTERLOCK
BATTERY
RADIO XMTR
TTY KBD
TTY PRINTER
RADIO RECVR
DELAY CORRECTOR
S2
OFF
SEND REC. RELAYS K11, K12 K4
S-R RELAY K7 CONTACTS
FF 39
S3 SPECIAL CHARACTER
G 12
FF38
CARD-I KW-9 DELAY CORRECTOR
SS9
SS10
G 46
P/o S6
ADVANCE
RETARD

FIG. 2. SN-228 (XC-2)/G, DETAILED BLOCK DIAGRAM.


P1001
16
-12V
C1008
150
R1036
2.4K
R1090
30K
CR1015
10
TO RELAY K12-8
C1009
11
TO CARD C-11 RELAY K12-4
R1037
30K
270
R1039
39K
CR1007
C1007
150
Q1014
Q1015
CR1006
R1038
39K
FF45
15
TO CARD C-14, D-18
13
+6V
12
TO CARD E-2, G-2
01
11-M
T
8
TO CARD B-1
R1081
27K
R1080
5K
R1082
30K
R1083
2.4K
R1084
30K
C1023
680
J1011
TEST JACK
C1022
680
R1079
20K
G-23
R1076
5K
CR1013
.47 µf
C1020
Q1028
Q1029
9
TO CARD F-10
R1077
6.8K
C1021
4700
R1078
100
R1085
10K
R1091
30K
14
GRD
CR1014
1N429

MAIN SIGNAL INTEGRATOR (CARD J), SCHEMATIC DIAGRAM.

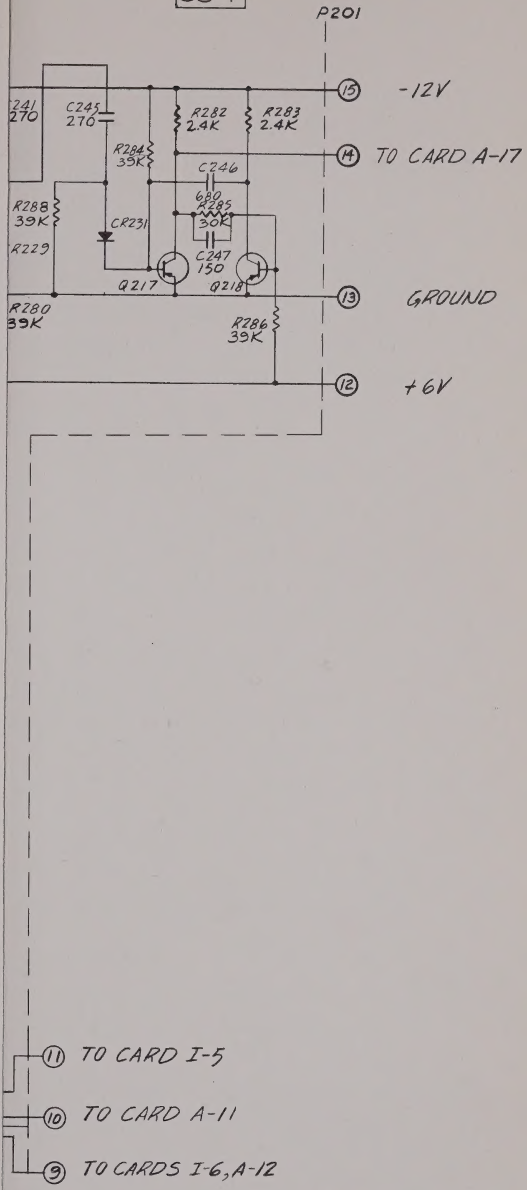

TO CARDS E-3 D-16, G-3
5
P1001
16 -12V
10 TO RELAY K12-8
11 TO CARD C-11 RELAY K12-4
15 TO CARD C-14, D-18
13 +6V
12 TO CARD E-2, G-2
8 TO CARD B-1
J1011 TEST JACK
G-23
9 TO CARD F-10
14 GRD
R1002 22K
R1003 5K
R1004 1K
R1007 5K
Q1028 2N388
R1092 56K
C1026 22μf
R1093 5K
Q1004
Q1002
R1006 10K
Q1001
Q1003
R1001 200
R1005 200
R1008 10K
2N388 Q1005
CR1001 1N457
60WPM
100WPM
NOTE 4
SPEED CHANGE JUMPER
R1009 4.22K
R1010 3.92K
R1012 2.43K
R1011 2.61K
C1001 2.2μf
R1013 316
CR1002 1N457
CR1003 1N457
CR1004
R1014 316
R1015 261
R1016 121
Q1007
Q1008
Q1006
R1017 56K
R1018 10K
R1020 5K
R1019 5K
Q1009
C1002 680
R1021 1.5K
R1022 220
R1023 1K
Q1010
R1024 10K
C1003 680
R1026 7.5K
R1025 5K
Q1011
Q1012
R1027 2.4K
R1028 30K
C1004 680
Q1013
R1030 39K
R1029 2.4K
C1005 270
R1031 30K
R1032 39K
CR1005
R1033 39K
R1035 2.4K
C1008 150
R1090 30K
R1037 30K
C1007 150
R1036 2.4K
Q1014
Q1015
R1038 39K
C1009 270
R1039 39K
CR1007
CR1015
CR1006
FF45
CR1012 1N753
R1045 5K
CR1009 1N457
Q1017
R1041 19.6K
R1042 18.2K
R1043 11.8K
R1044 11K
C1010 4.7μf
Q1016
CR1008 1N457
R1040 10K
R1046 30K
Q1018
R1047 39K
R1048 20K
CR1010 1N457
C1011 22μf
R1049 100K
R1050 5K
C1024 4.7μf
Q1019
R1051 20K
R1052 22K
R1053 1K
C1012 60μf
R1054 30K
CR1011
Q1020
R1055 2.4K
C1014 4.7μf
R1057 30K
C1013 270
R1056 30K
R1058 2.4K
Q1021
2N388
Q1022
R1059 39K
R1060 10K
2N466
C1025 10μf
Q1023
C1015 10μf
R1061 100K
R1062 10K
R1063 5K
R1064 18K
R1065 12K
Q1024 2N466
R1066 5.6K
R1050 5.6K
C1016 10μf
R1068 6.2K
Q1026 2N466
Q1025 2N466
R1069 11K
C1017 10μf
R1067 130
R1070 470
R1073 510
C1018 10μf
R1071 3.9K
T1001 MMT11-M
L1001 .25hy
C1027 4700
2N158 Q1027
R1072 150
C1019 10μf
R1075 51
R1074 1.0
R1076 5K
.47μf C1020
R1077 6.8K
R1081 27K
C1021 4700
R1078 100
Q1028
R1080 5K
C1023 680
R1079 20K
R1082 30K
R1083 2.4K
R1084 30K
C1022 680
Q1029
CR1013
R1091 30K
R1085 10K
SPEED CHANGE JUMPER
60WPM
100WPM
R1089 TRIM 10K
R1087 5.6K
R1088 TRIM 10K
R1086 5.6K
CR1014 1N429
FORK INPUT
FORK OUTPUT
1 TO FEED THRU C-9
2 TO CARD A-7
3 TO INDICATOR I 2
4 TO CARD H-7
6 TO TUNING FORK OVEN
7

NOTES:

1. UNLESS OTHERWISE NOTED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN UUF.
   TRANSISTORS: 2N404
   DIODES: IN198
2. ⑤ INDICATES CONNECTOR PIN.
3. LETTER AND NUMBER COMBINATION INDICATES CARD AND PIN.
4. PROPER RESISTOR SELECTED BY MANUFACTURER.

FIG. 3. TUNING FORK OSCILLATOR AND MAIN SIGNAL INTEGRATOR (CARD J), SCHEMATIC DIAGRAM.

SS-1


P201
241
270
C245
270
R282
2.4K
R283
2.4K
R284
39K
C246
680
R285
30K
R288
39K
CR231
R229
C247
150
Q217
Q218
R280
39K
R286
39K
15 -12V
14 TO CARD A-17
13 GROUND
12 +6V
11 TO CARD I-5
10 TO CARD A-11
9 TO CARDS I-6, A-12

CORRECTOR (CARD B), SCHEMATIC DIAGRAM.

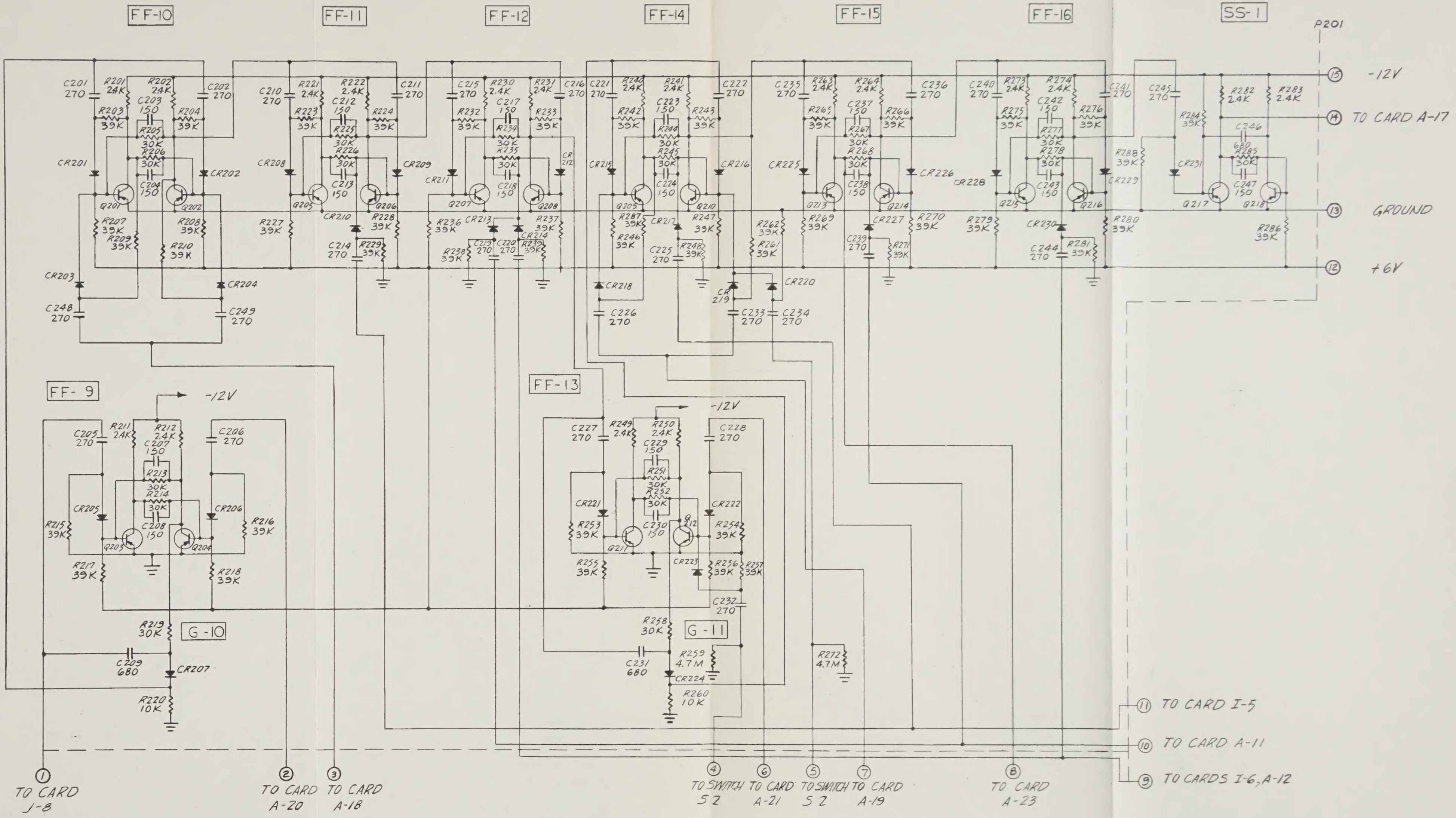

FF-10
FF-11
FF-12
FF-14
FF-15
FF-16
SS-1
P201
FF-9
FF-13
G-10
G-11
-12V
-12V
-12V
15 -12V
14 TO CARD A-17
13 GROUND
12 +6V
11 TO CARD I-5
10 TO CARD A-11
9 TO CARDS I-6, A-12
1 TO CARD J-8
2 TO CARD A-20
3 TO CARD A-18
4 TO SWITCH S2
6 TO CARD A-21
5 TO SWITCH S2
7 TO CARD A-19
8 TO CARD A-23
Q201
Q202
Q203
Q204
Q205
Q206
Q207
Q208
Q209
Q210
Q211
Q212
Q213
Q214
Q215
Q216
Q217
Q218
C201 270
C202 270
C203 150
C204 150
C205 270
C206 270
C207 150
C208 150
C209 680
C231 680
C246 680
R201 2.4K
R202 2.4K
R203 39K
R204 39K
R205 30K
R206 30K
R219 30K
R220 10K
R258 30K
R259 4.7M
R260 10K
R272 4.7M
CR201
CR202
CR203
CR204
CR207
CR224
C248 270
C249 270
C232 270

FIG. 4. BINARY DIVIDER AND PHASE CORRECTOR (CARD B), SCHEMATIC DIAGRAM.

NOTES:

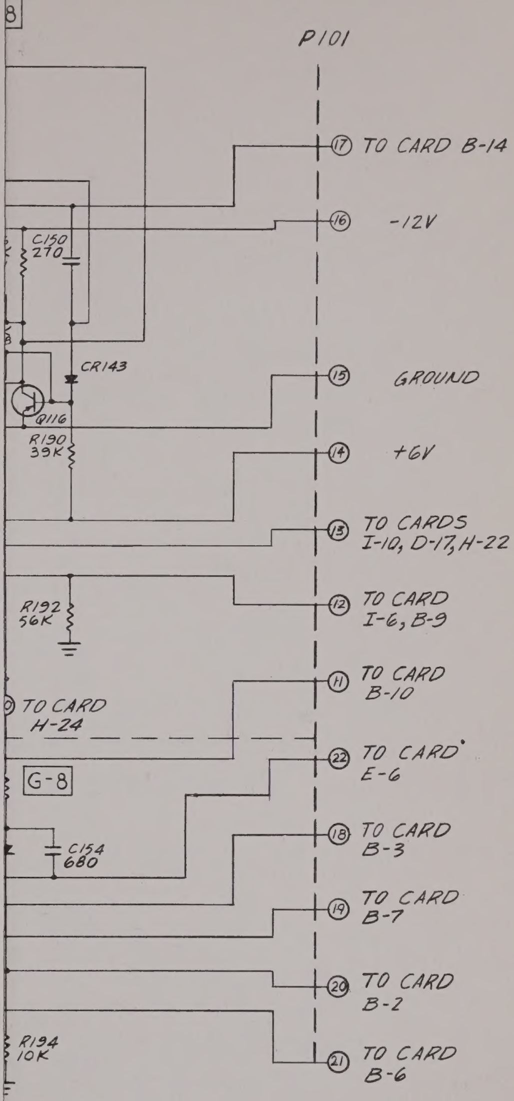
1. UNLESS OTHERWISE NOTED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN UUF.

   TRANSISTORS: 2N404

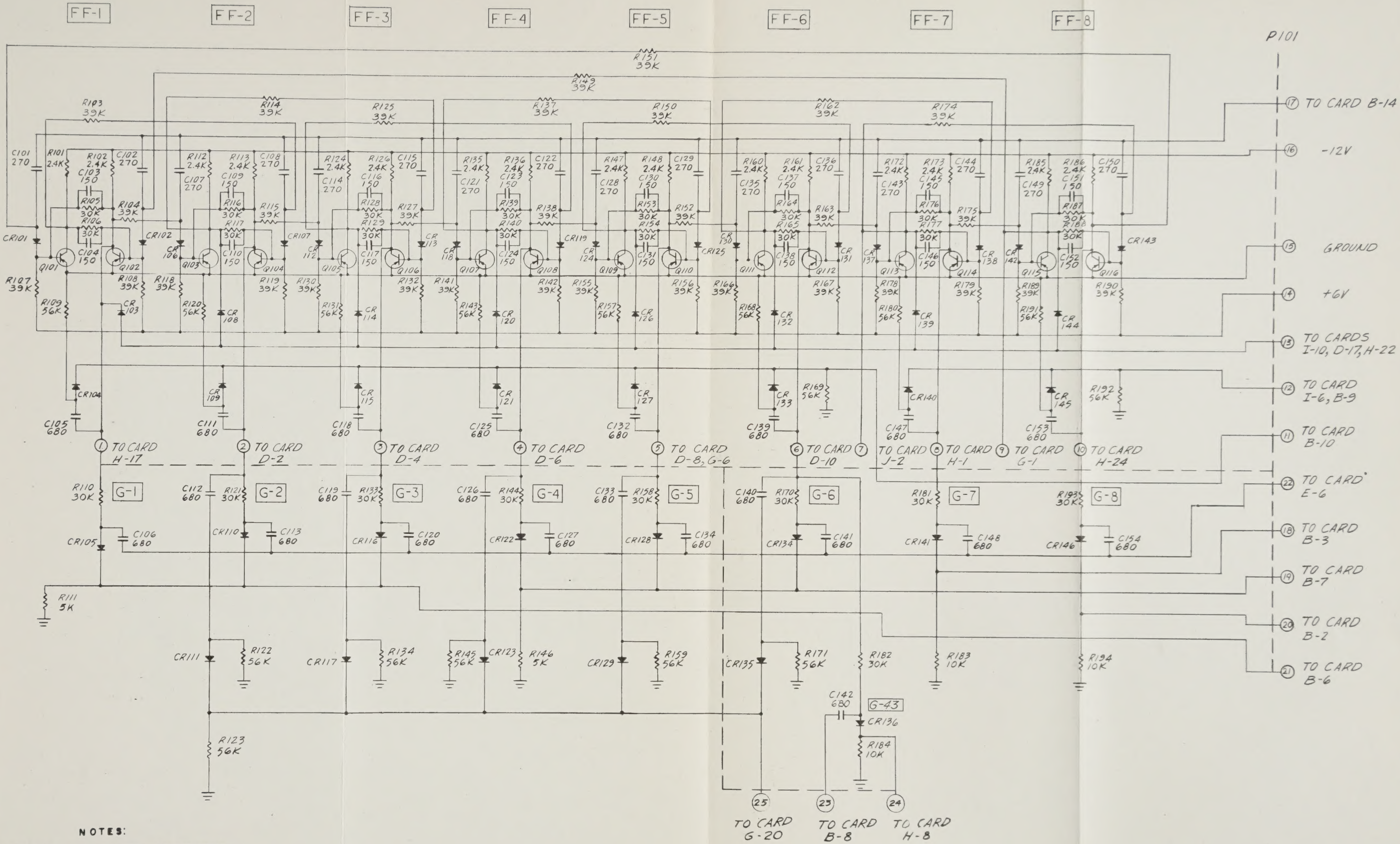
   DIODES: IN198

2. ⑤ INDICATES CONNECTOR PIN.

3. LETTER AND NUMBER COMBINATION INDICATES CARD AND PIN.


8
P101
17 TO CARD B-14
16 -12V
C150
270
CR143
Q116
15 GROUND
R190
39K
14 +6V
13 TO CARDS I-10, D-17, H-22
R192
56K
12 TO CARD I-6, B-9
11 TO CARD B-10
TO CARD H-24
22 TO CARD E-6
G-8
C154
680
18 TO CARD B-3
19 TO CARD B-7
20 TO CARD B-2
R194
10K
21 TO CARD B-6

TOR (CARD A), SCHEMATIC DIAGRAM.


FF-1
FF-2
FF-3
FF-4
FF-5
FF-6
FF-7
FF-8
P101
17 TO CARD B-14
16 -12V
15 GROUND
14 +6V
13 TO CARDS I-10, D-17, H-22
12 TO CARD I-6, B-9
11 TO CARD B-10
22 TO CARD E-6
18 TO CARD B-3
19 TO CARD B-7
20 TO CARD B-2
21 TO CARD B-6
1 TO CARD H-17
2 TO CARD D-2
3 TO CARD D-4
4 TO CARD D-6
5 TO CARD D-8, G-6
6 TO CARD D-10
7 TO CARD J-2
8 TO CARD H-1
9 TO CARD G-1
10 TO CARD H-24
G-1
G-2
G-3
G-4
G-5
G-6
G-7
G-8
G-43
25 TO CARD G-20
23 TO CARD B-8
24 TO CARD H-8

NOTES:

1. UNLESS OTHERWISE NOTED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN UUF.

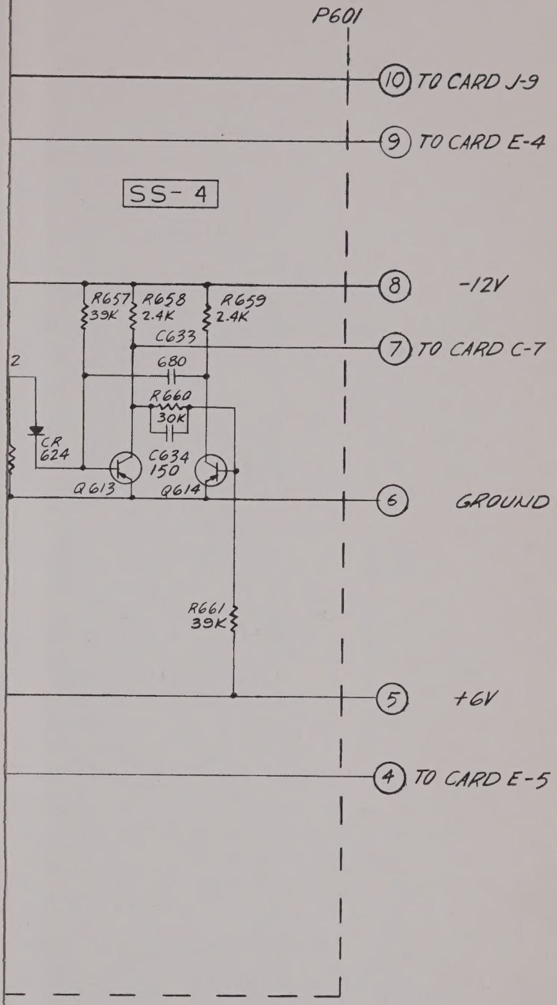
   TRANSISTORS: 2N404

   DIODES: IN198

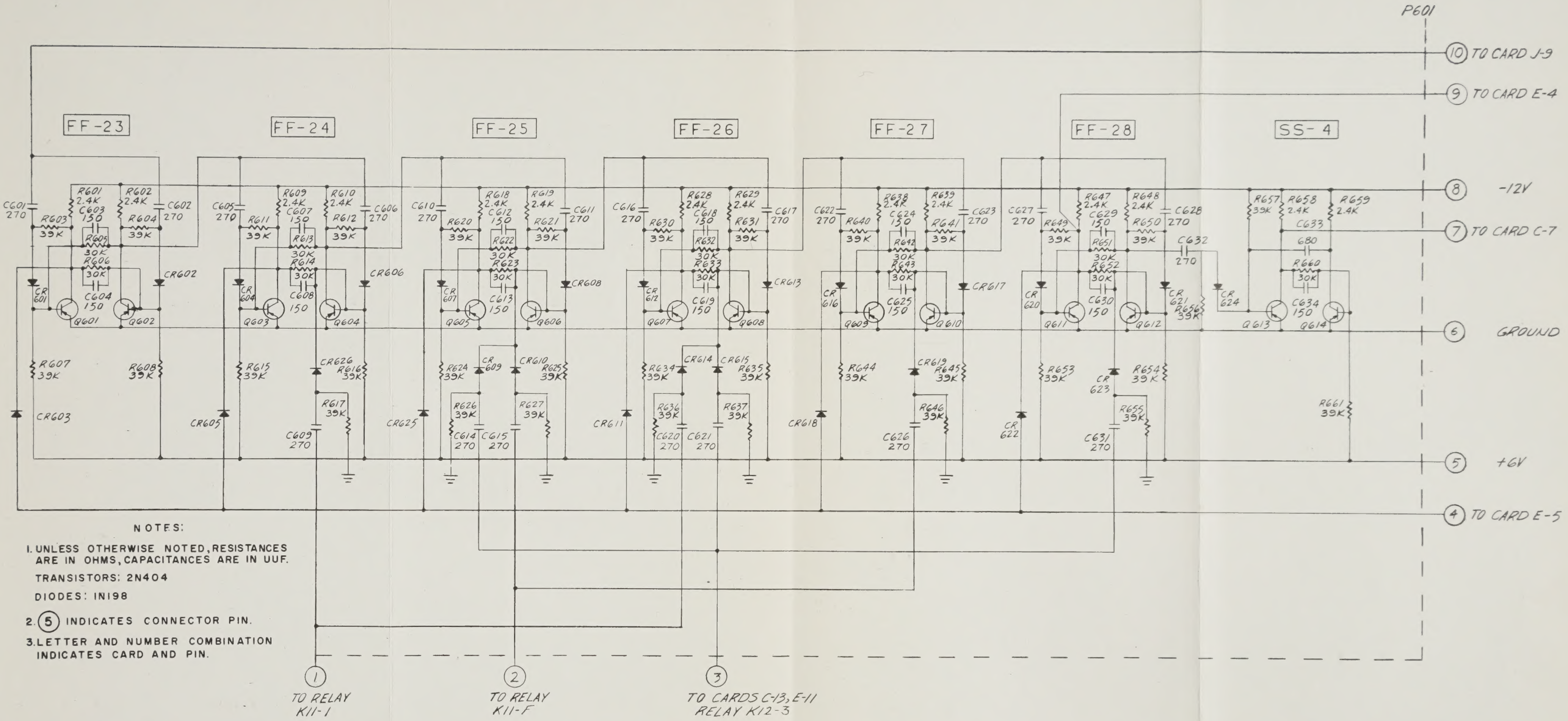
2. ⑤ INDICATES CONNECTOR PIN.

3. LETTER AND NUMBER COMBINATION INDICATES CARD AND PIN.

FIG. 5. CHARACTER REGENERATOR (CARD A), SCHEMATIC DIAGRAM.


P601
10
TO CARD J-9
9
TO CARD E-4
SS- 4
8
-12V
R657
39K
R658
2.4K
R659
2.4K
C633
680
7
TO CARD C-7
2
R660
30K
C634
150
CR
624
Q613
Q614
6
GROUND
R661
39K
5
+6V
4
TO CARD E-5

(CARD F), SCHEMATIC DIAGRAM.


P601
(10) TO CARD J-9
(9) TO CARD E-4
(8) -12V
(7) TO CARD C-7
(6) GROUND
(5) +6V
(4) TO CARD E-5
FF-23
FF-24
FF-25
FF-26
FF-27
FF-28
SS-4
C601 270
R601 2.4K
R602 2.4K
C602 270
R603 39K
C603 150
R604 39K
R605 30K
R606 30K
C604 150
CR601
Q601
Q602
CR602
R607 39K
R608 39K
CR603
C605 270
R609 2.4K
R610 2.4K
C606 270
R611 39K
C607 150
R612 39K
R613 30K
R614 30K
C608 150
CR604
Q603
Q604
CR606
R615 39K
CR626
R616 39K
R617 39K
C609 270
CR605
C610 270
R618 2.4K
R619 2.4K
C611 270
R620 39K
C612 150
R621 39K
R622 30K
R623 30K
C613 150
CR607
Q605
Q606
CR608
R624 39K
CR609
CR610
R625 39K
R626 39K
R627 39K
C614 270
C615 270
CR625
C616 270
R628 2.4K
R629 2.4K
C617 270
R630 39K
C618 150
R631 39K
R632 30K
R633 30K
C619 150
CR612
Q607
Q608
CR613
R634 39K
CR614
CR615
R635 39K
R636 39K
R637 39K
C620 270
C621 270
CR611
C622 270
R638 2.4K
R639 2.4K
C623 270
R640 39K
C624 150
R641 39K
R642 30K
R643 30K
C625 150
CR616
Q609
Q610
CR617
R644 39K
CR619
R645 39K
R646 39K
C626 270
CR618
C627 270
R647 2.4K
R648 2.4K
C628 270
R649 39K
C629 150
R650 39K
R651 30K
R652 30K
C630 150
C632 270
CR620
Q611
Q612
CR621
R656 39K
CR624
R653 39K
CR623
R654 39K
R655 39K
C631 270
CR622
R657 39K
R658 2.4K
R659 2.4K
C633 680
R660 30K
C634 150
Q613
Q614
R661 39K
(1) TO RELAY K11-1
(2) TO RELAY K11-F
(3) TO CARDS C-13, E-11 RELAY K12-3

NOTES:

1. UNLESS OTHERWISE NOTED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN UUF.

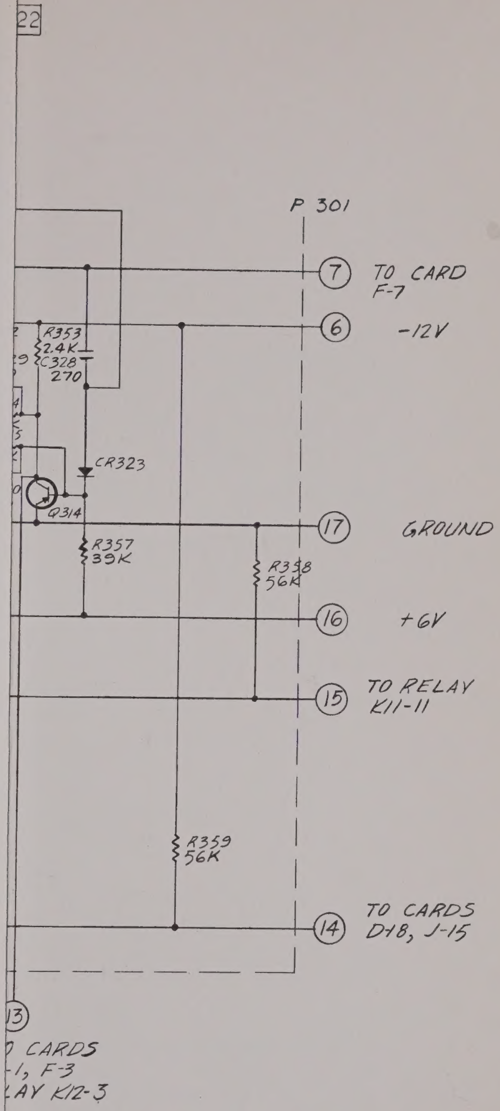
   TRANSISTORS: 2N404

   DIODES: IN198

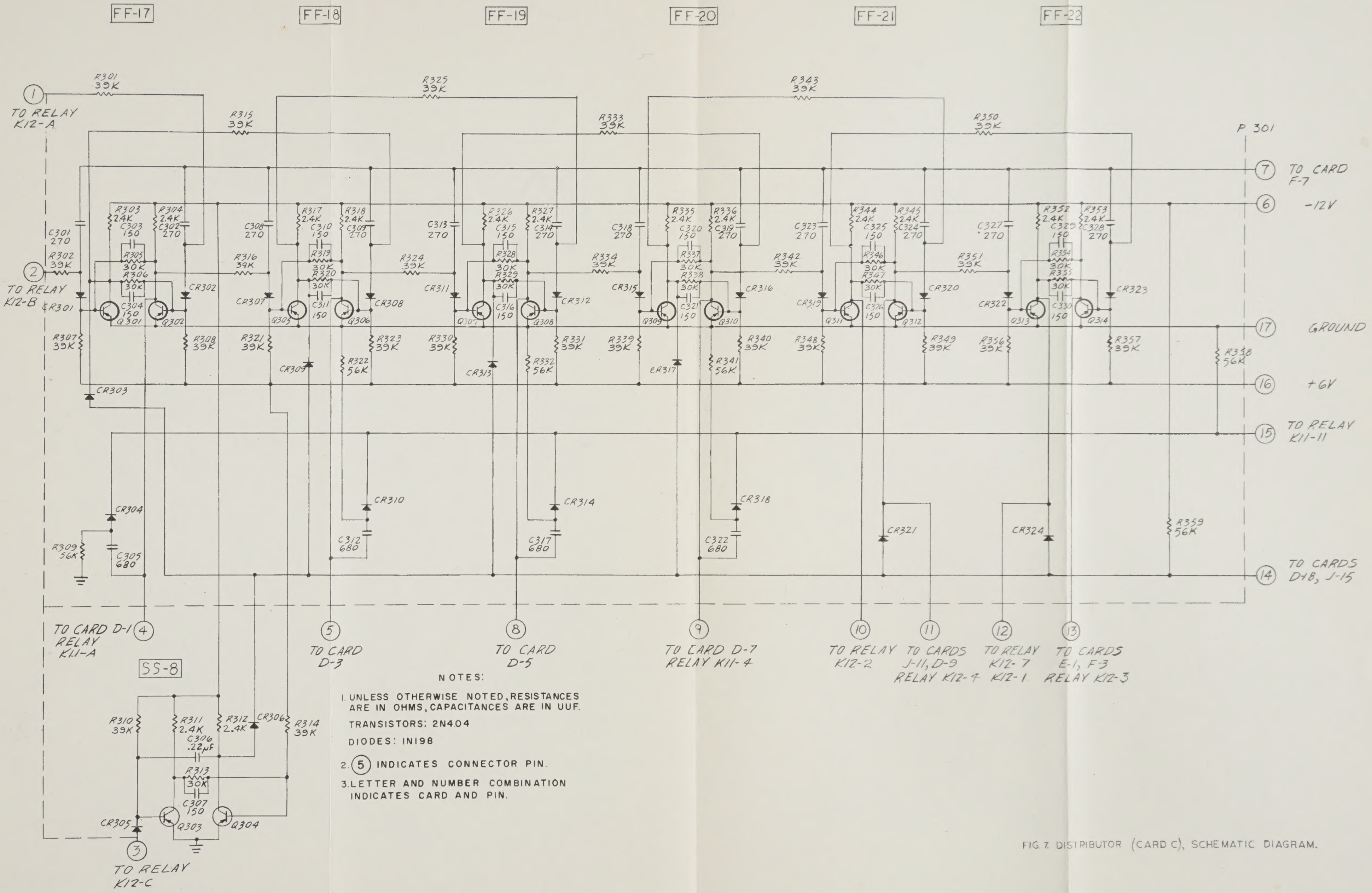
2. ⑤ INDICATES CONNECTOR PIN.

3. LETTER AND NUMBER COMBINATION INDICATES CARD AND PIN.

FIG. 6. BINARY DIVIDER (CARD F), SCHEMATIC DIAGRAM.


22
P 301
7
TO CARD F-7
6
-12V
R353
2.4K
C328
270
CR323
Q314
17
GROUND
R357
39K
R358
56K
16
+6V
15
TO RELAY K11-11
R359
56K
14
TO CARDS D-18, J-15
13
CARDS
-1, F-3
AY K12-3

STRIBUTOR (CARD C), SCHEMATIC DIAGRAM.


FF-17
FF-18
FF-19
FF-20
FF-21
FF-22
SS-8
R301 39K
R325 39K
R343 39K
R315 39K
R333 39K
R350 39K
P 301
① TO RELAY K12-A
② TO RELAY K12-B
R303 2.4K
R304 2.4K
C303 150
C302 270
C301 270
R302 39K
R305 30K
R306 30K
C304 150
CR301
CR302
Q301
Q302
R307 39K
R308 39K
CR303
C308 270
R316 39K
CR307
R317 2.4K
R318 2.4K
C310 150
C309 270
R319
R320 30K
C311 150
Q305
Q306
CR308
R321 39K
R322 56K
R323 39K
CR309
R324 39K
C313 270
CR311
R326 2.4K
R327 2.4K
C315 150
C314 270
R328 30K
R329 30K
C316 150
Q307
Q308
CR312
R330 39K
R331 39K
R332 56K
CR313
R334 39K
C318 270
CR315
R335 2.4K
R336 2.4K
C320 150
C319 270
R337 30K
R338 30K
C321 150
Q309
Q310
CR316
R339 39K
R340 39K
R341 56K
CR317
R342 39K
C323 270
CR319
R344 2.4K
R345 2.4K
C325 150
C324 270
R346 30K
R347 30K
C326 150
Q311
Q312
CR320
R348 39K
R349 39K
R351 39K
C327 270
CR322
R352 2.4K
R353 2.4K
C329 150
C328 270
R354 30K
R355 30K
C330 150
Q313
Q314
CR323
R356 39K
R357 39K
R358 56K
⑦ TO CARD F-7
⑥ -12V
⑰ GROUND
⑯ +6V
⑮ TO RELAY K11-11
⑭ TO CARDS D+8, J-15
CR304
R309 56K
C305 680
CR310
C312 680
CR314
C317 680
CR318
C322 680
CR321
CR324
R359 56K
④ TO CARD D-1 RELAY K11-A
⑤ TO CARD D-3
⑧ TO CARD D-5
⑨ TO CARD D-7 RELAY K11-4
⑩ TO RELAY K12-2
⑪ TO CARDS J-11, D-9 RELAY K12-4
⑫ TO RELAY K12-7 K12-1
⑬ TO CARDS E-1, F-3 RELAY K12-3
R310 39K
R311 2.4K
R312 2.4K
CR306
R314 39K
C306 .22μF
R313 30K
C307 150
CR305
Q303
Q304
③ TO RELAY K12-C

NOTES:

1. UNLESS OTHERWISE NOTED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN UUF.

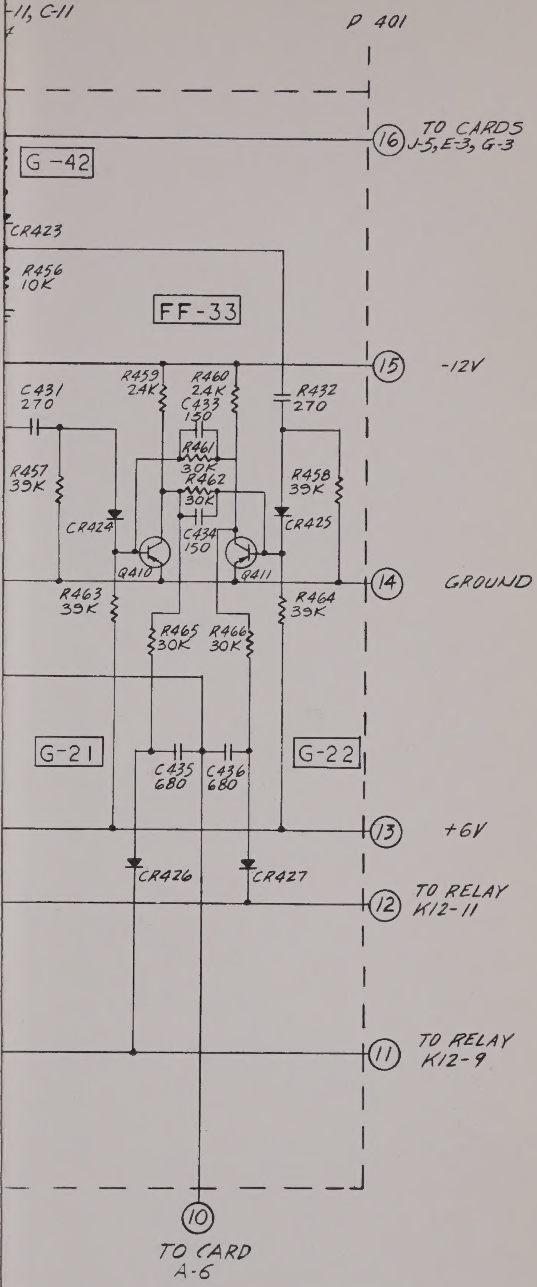
TRANSISTORS: 2N404

DIODES: IN198

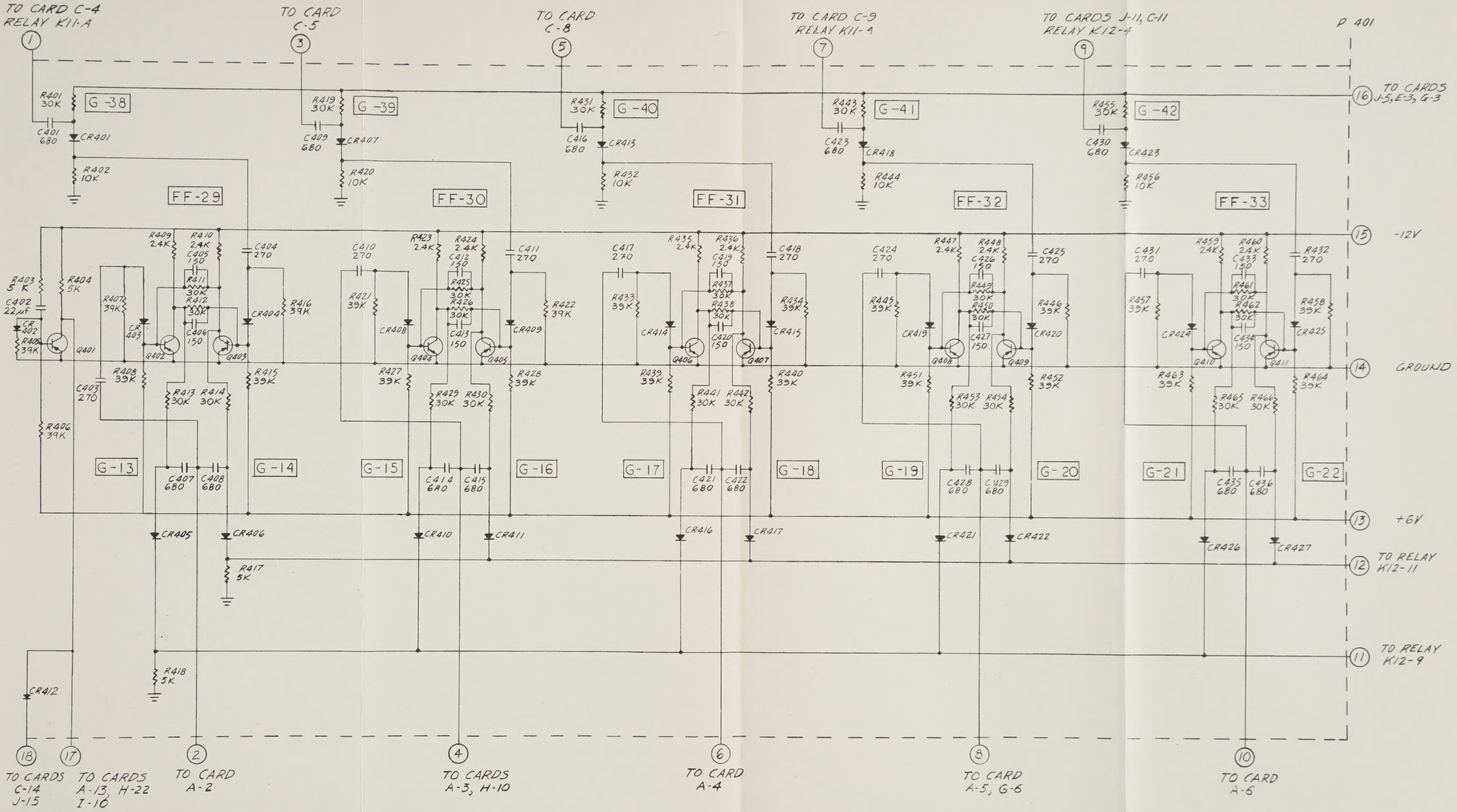
2. ⑤ INDICATES CONNECTOR PIN.

3. LETTER AND NUMBER COMBINATION INDICATES CARD AND PIN.

FIG. 7. DISTRIBUTOR (CARD C), SCHEMATIC DIAGRAM.


-11, C-11
P 401
16
TO CARDS J-5, E-3, G-3
G -42
CR423
R456 10K
FF-33
15
-12V
C431 270
R459 24K
R460 24K
C433 150
R432 270
R461 30K
R462 30K
R457 39K
R458 39K
CR424
CR425
C434 150
Q410
Q411
14
GROUND
R463 39K
R464 39K
R465 30K
R466 30K
G-21
G-22
C435 680
C436 680
13
+6V
CR426
CR427
12
TO RELAY K12-11
11
TO RELAY K12-9
10
TO CARD A-6

R(CARD D), SCHEMATIC DIAGRAM.


TO CARD C-4 RELAY K11-A
1
TO CARD C-5
3
TO CARD C-8
5
TO CARD C-9 RELAY K11-4
7
TO CARDS J-11, C-11 RELAY K12-4
9
P 401
16
TO CARDS J-5, E-3, G-3
15
-12V
14
GROUND
13
+6V
12
TO RELAY K12-11
11
TO RELAY K12-9
G-38
G-39
G-40
G-41
G-42
FF-29
FF-30
FF-31
FF-32
FF-33
G-13
G-14
G-15
G-16
G-17
G-18
G-19
G-20
G-21
G-22
R401 30K
C401 680
CR401
R402 10K
R419 30K
C409 680
CR407
R420 10K
R431 30K
C416 680
CR413
R432 10K
R443 30K
C423 680
CR418
R444 10K
R455 30K
C430 680
CR423
R456 10K
R403 5K
C402 22μf
CR402
R405 39K
R404 5K
Q401
R406 39K
R407 39K
CR403
R408 39K
C403 270
Q402
R409 2.4K
R410 2.4K
C405 150
R411 30K
R412 30K
C406 150
Q403
C404 270
CR404
R416 39K
R415 39K
R413 30K
R414 30K
C407 680
C408 680
CR405
CR406
R417 5K
R418 5K
CR412
C410 270
R421 39K
CR408
Q404
R423 2.4K
R424 2.4K
C412 150
R425 30K
R426 30K
C413 150
Q405
C411 270
CR409
R422 39K
R427 39K
R428 39K
R429 30K
R430 30K
C414 680
C415 680
CR410
CR411
C417 270
R433 39K
CR414
Q406
R435 2.4K
R436 2.4K
C419 150
R437 30K
R438 30K
C420 150
Q407
C418 270
CR415
R434 39K
R439 39K
R440 39K
R441 30K
R442 30K
C421 680
C422 680
CR416
CR417
C424 270
R445 39K
CR419
Q408
R447 2.4K
R448 2.4K
C426 150
R449 30K
R450 30K
C427 150
Q409
C425 270
CR420
R446 39K
R451 39K
R452 39K
R453 30K
R454 30K
C428 680
C429 680
CR421
CR422
C431 270
R457 39K
CR424
Q410
R459 2.4K
R460 2.4K
C433 150
R461 30K
R462 30K
C434 150
Q411
R432 270
CR425
R458 39K
R463 39K
R464 39K
R465 30K
R466 30K
C435 680
C436 680
CR426
CR427
18
TO CARDS C-14 J-15
17
TO CARDS A-13, H-22 I-10
2
TO CARD A-2
4
TO CARDS A-3, H-10
6
TO CARD A-4
8
TO CARD A-5, G-6
10
TO CARD A-6

NOTES:

1. UNLESS OTHERWISE NOTED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN UUF.

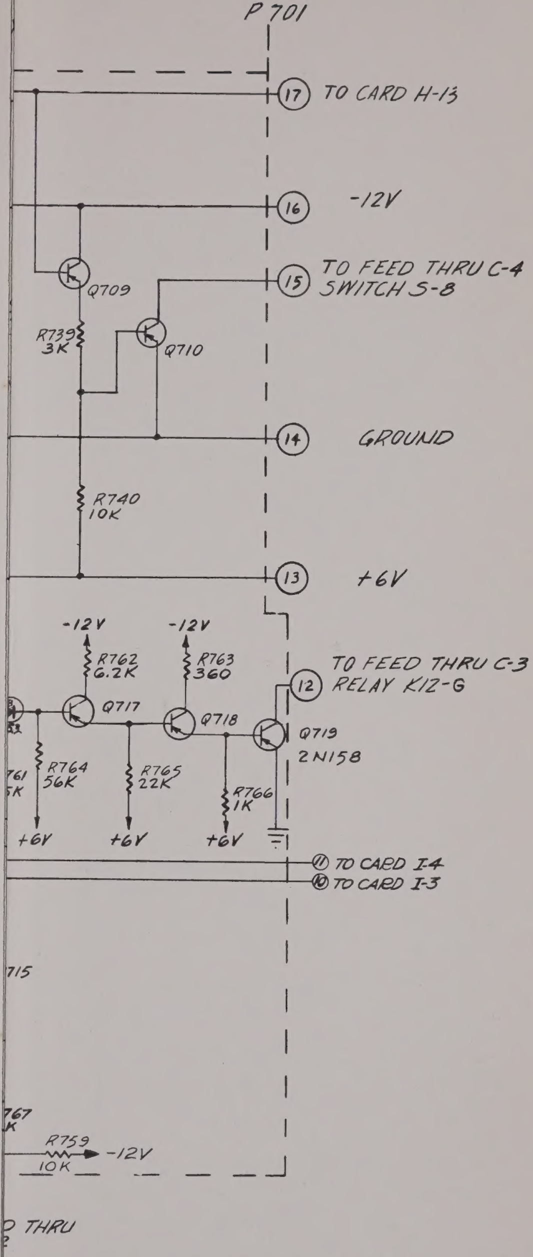
TRANSISTORS: 2N404

DIODES: IN198

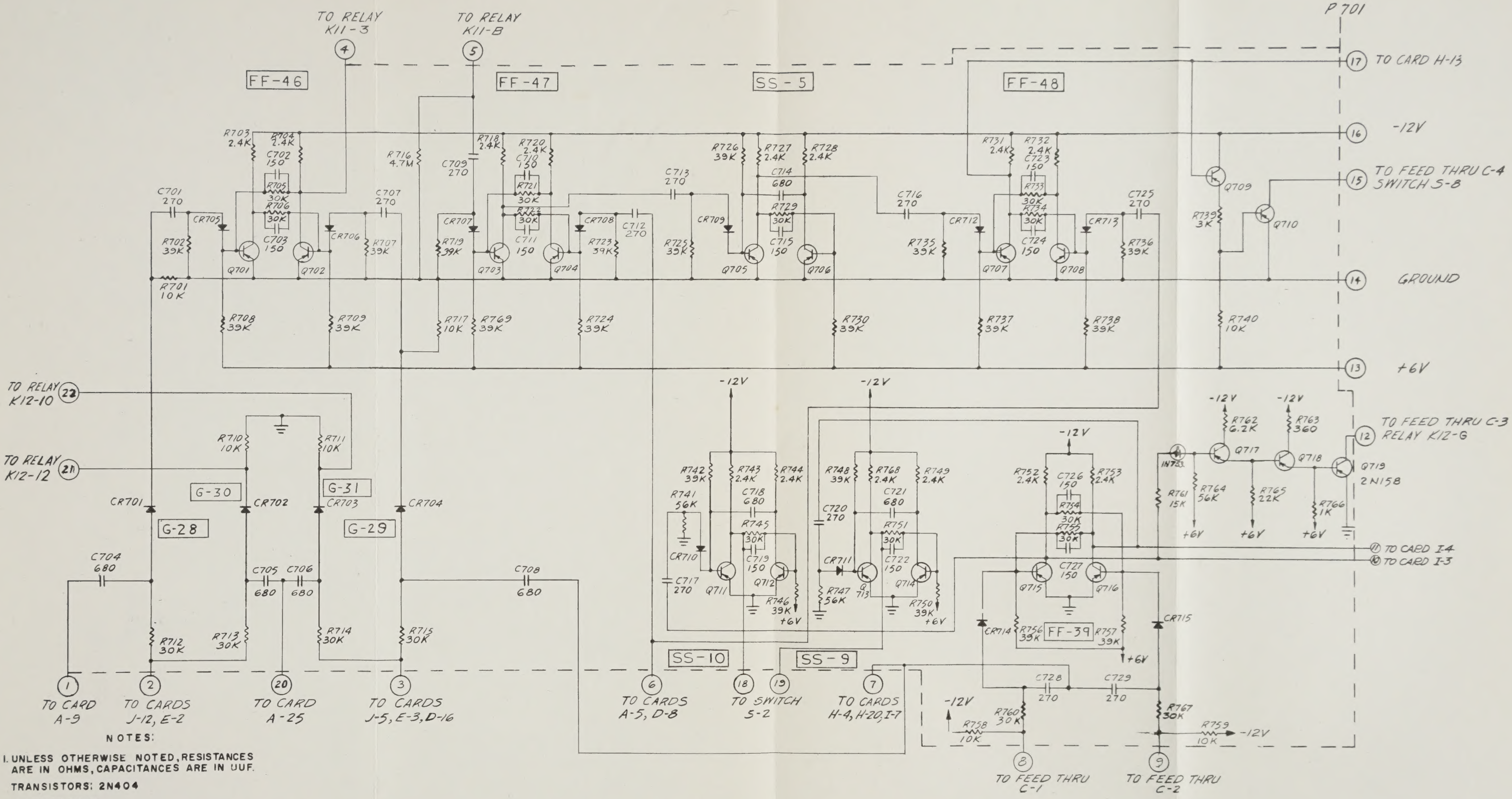
2. ⑤ INDICATES CONNECTOR PIN.

3. LETTER AND NUMBER COMBINATION INDICATES CARD AND PIN.

FIG.8. EXTENSOR (CARD D), SCHEMATIC DIAGRAM.


P701
17
TO CARD H-13
16
-12V
15
TO FEED THRU C-4
SWITCH S-8
Q709
R739
3K
Q710
14
GROUND
R740
10K
13
+6V
-12V
-12V
R762
6.2K
R763
360
12
TO FEED THRU C-3
RELAY K12-G
Q717
Q718
Q719
2N158
761
K
R764
56K
R765
22K
R766
1K
+6V
+6V
+6V
⑪ TO CARD I-4
⑩ TO CARD I-3
715
767
K
R759
10K
-12V
O THRU

(CARD G), SCHEMATIC DIAGRAM.


TO RELAY K11-3
4
TO RELAY K11-B
5
P701
FF-46
FF-47
SS-5
FF-48
17 TO CARD H-13
16 -12V
15 TO FEED THRU C-4 SWITCH S-8
14 GROUND
13 +6V
12 TO FEED THRU C-3 RELAY K12-G
R703 2.4K
R704 2.4K
C702 150
R705 30K
R706 30K
C703 150
C701 270
R702 39K
R701 10K
CR705
Q701
Q702
CR706
C707 270
R707 39K
R708 39K
R709 39K
R716 4.7M
C709 270
R718 2.4K
R720 2.4K
C710 150
R721 30K
R722 30K
C711 150
CR707
R719 39K
Q703
Q704
CR708
R723 39K
C712 270
R717 10K
R769 39K
R724 39K
C713 270
R726 39K
R727 2.4K
R728 2.4K
C714 680
R729 30K
C715 150
CR709
R725 39K
Q705
Q706
R730 39K
C716 270
R731 2.4K
R732 2.4K
C723 150
R733 30K
R734 30K
C724 150
CR712
R735 39K
Q707
Q708
CR713
C725 270
R736 39K
R737 39K
R738 39K
Q709
Q710
R739 3K
R740 10K
TO RELAY K12-10
22
TO RELAY K12-12
21
R710 10K
R711 10K
G-30
G-31
G-28
G-29
CR701
CR702
CR703
CR704
C704 680
C705 680
C706 680
C708 680
R712 30K
R713 30K
R714 30K
R715 30K
-12V
R742 39K
R743 2.4K
R744 2.4K
R741 56K
C718 680
R745 30K
C719 150
CR710
C717 270
Q711
Q712
R746 39K
+6V
R748 39K
R768 2.4K
R749 2.4K
C720 270
C721 680
R751 30K
C722 150
CR711
Q713
Q714
R747 56K
R750 39K
SS-10
SS-9
R752 2.4K
C726 150
R753 2.4K
R754 30K
R755 30K
Q715
C727 150
Q716
CR714
R756 39K
FF-39
R757 39K
CR715
R762 6.2K
R763 360
Q717
Q718
Q719 2N158
1N753
R761 15K
R764 56K
R765 22K
R766 1K
11 TO CARD I-4
10 TO CARD I-3
C728 270
C729 270
R760 30K
R758 10K
R767 30K
R759 10K
1 TO CARD A-9
2 TO CARDS J-12, E-2
20 TO CARD A-25
3 TO CARDS J-5, E-3, D-16
6 TO CARDS A-5, D-8
18 TO SWITCH S-2
19
7 TO CARDS H-4, H-20, I-7
8 TO FEED THRU C-1
9 TO FEED THRU C-2

NOTES:

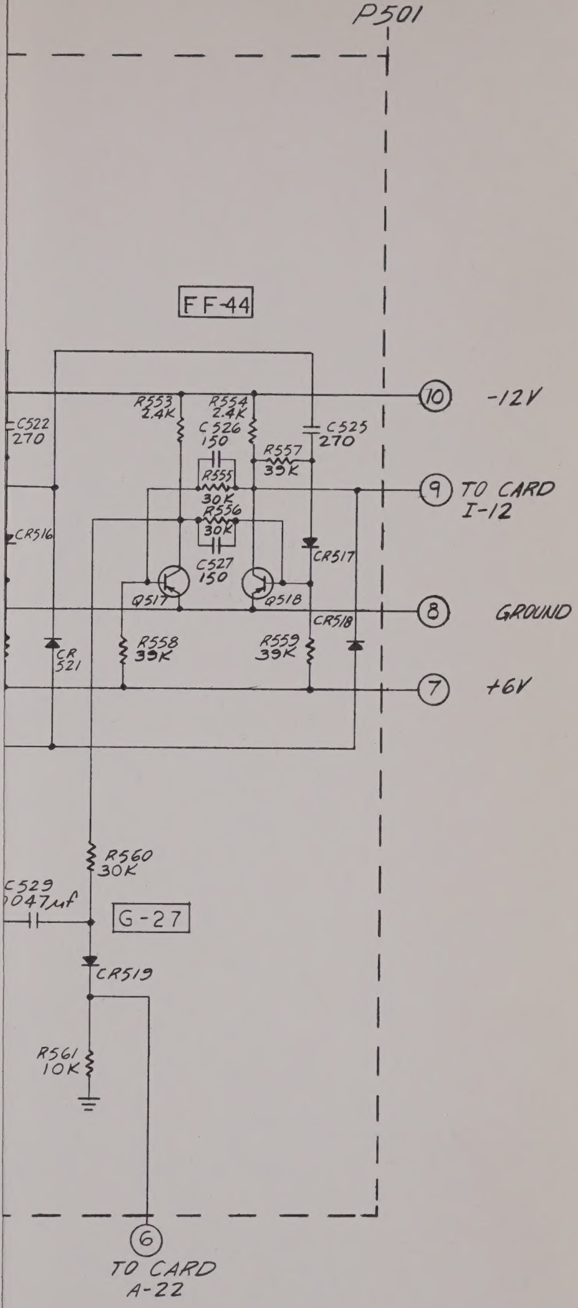
1. UNLESS OTHERWISE NOTED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN UUF.

   TRANSISTORS: 2N404

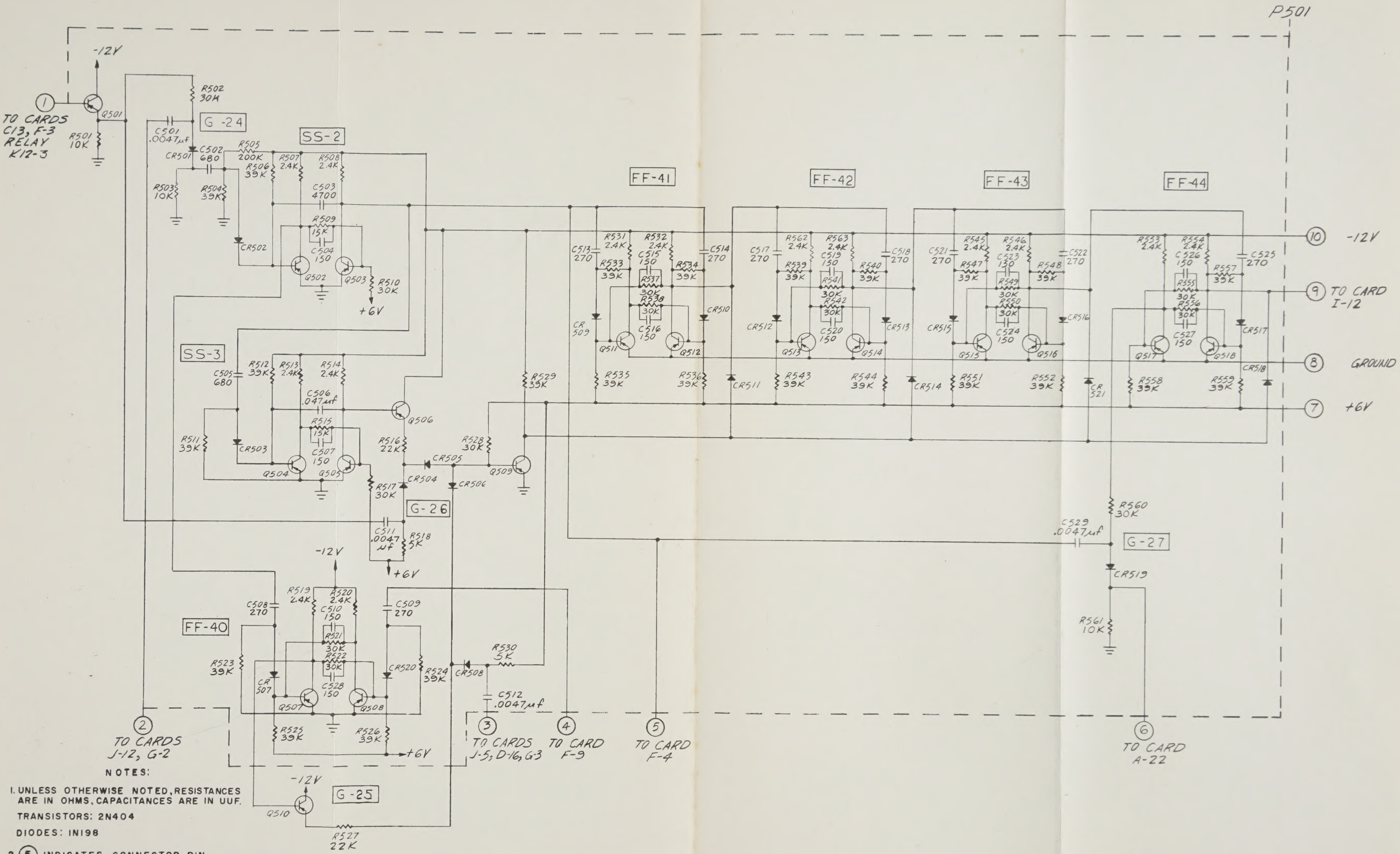
   DIODES: IN198

2. ⑤ INDICATES CONNECTOR PIN.
3. LETTER AND NUMBER COMBINATION INDICATES CARD AND PIN.

FIG.9. OUTPUT CONTROL (CARD G), SCHEMATIC DIAGRAM.


P501
FF-44
C522
270
R553
2.4K
R554
2.4K
C526
150
C525
270
R557
39K
R555
30K
R556
30K
C527
150
CR516
CR517
Q517
Q518
CR518
CR
521
R558
39K
R559
39K
10
-12V
9
TO CARD
I-12
8
GROUND
7
+6V
R560
30K
C529
.047μf
G-27
CR519
R561
10K
6
TO CARD
A-22

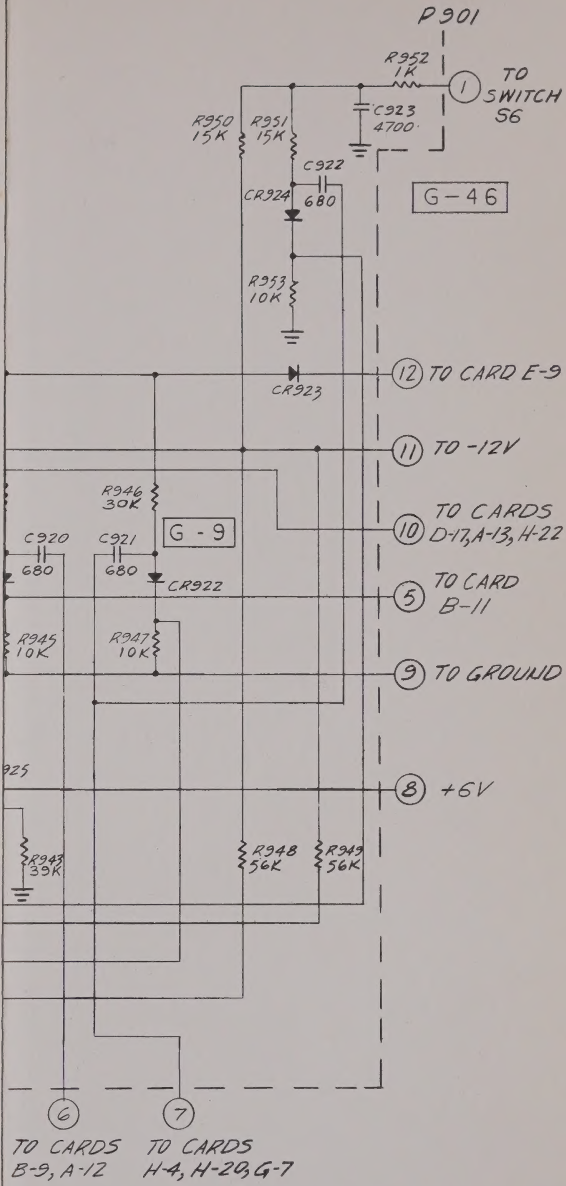
TOR (CARD E), SCHEMATIC DIAGRAM.


P501
-12V
① TO CARDS C13, F-3 RELAY K12-3
Q501
R501 10K
R502 30K
C501 .0047μf
G -24
SS-2
CR501
C502 680
R505 200K
R506 39K
R507 2.4K
R508 2.4K
R503 10K
R504 39K
C503 4700
R509 15K
C504 150
CR502
Q502
Q503
R510 30K
+6V
FF-41
FF-42
FF-43
FF-44
C513 270
R531 2.4K
R532 2.4K
C515 150
C514 270
R533 39K
R534 39K
R537 30K
R538 30K
C516 150
CR 509
CR510
Q511
Q512
R535 39K
R536 39K
CR511
C517 270
R562 2.4K
R563 2.4K
C519 150
C518 270
R539 39K
R540 39K
R541 30K
R542 30K
C520 150
CR512
CR513
Q513
Q514
R543 39K
R544 39K
CR514
C521 270
R545 2.4K
R546 2.4K
C523 150
C522 270
R547 39K
R548 39K
R549 30K
R550 30K
C524 150
CR515
CR516
Q515
Q516
R551 39K
R552 39K
CR 521
R553 2.4K
R554 2.4K
C526 150
C525 270
R557 39K
R555 30K
R556 30K
C527 150
CR517
CR518
Q517
Q518
R558 39K
R559 39K
⑩ -12V
⑨ TO CARD I-12
⑧ GROUND
⑦ +6V
SS-3
C505 680
R512 39K
R513 2.4K
R514 2.4K
C506 .047μf
R515 15K
C507 150
R511 39K
CR503
Q504
Q505
Q506
R516 22K
R517 30K
CR504
CR505
CR506
R528 30K
R529 39K
Q509
G- 26
C511 .0047 μf
R518 5K
+6V
R560 30K
C529 .0047μf
G - 27
CR519
R561 10K
-12V
FF-40
C508 270
R519 2.4K
R520 2.4K
C510 150
C509 270
R521 30K
R522 30K
C528 150
R523 39K
R524 39K
CR 507
CR520
Q507
Q508
R525 39K
R526 39K
+6V
R530 5K
CR508
C512 .0047μf
② TO CARDS J-12, G-2
③ TO CARDS J-5, D-16, G-3
④ TO CARD F-9
⑤ TO CARD F-4
⑥ TO CARD A-22
-12V
Q510
G -25
R527 22K

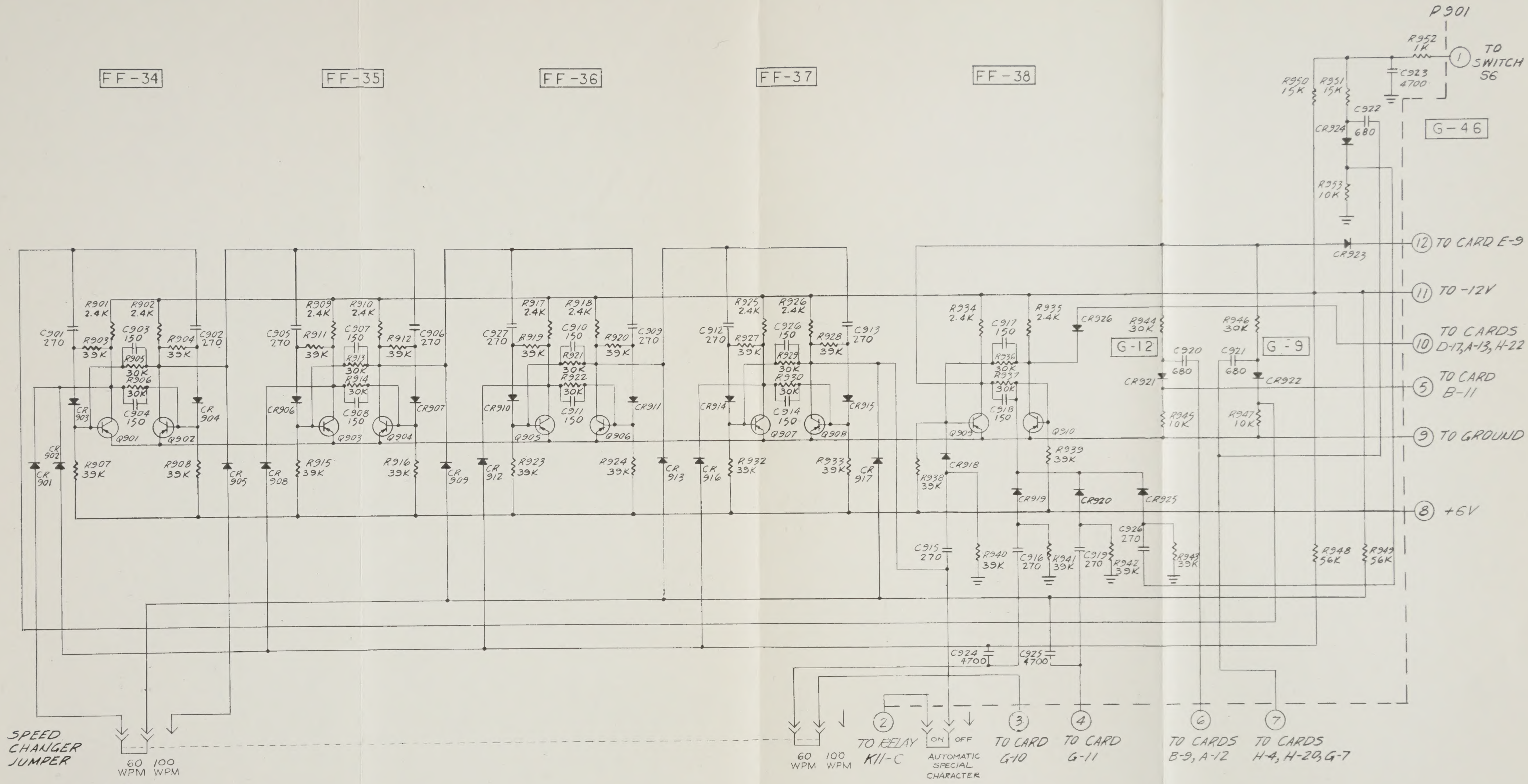
NOTES:

1. UNLESS OTHERWISE NOTED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN UUF.
   TRANSISTORS: 2N404
   DIODES: IN198
2. ⑤ INDICATES CONNECTOR PIN.
3. LETTER AND NUMBER COMBINATION INDICATES CARD AND PIN.

FIG. 10. EXTRACTOR (CARD E), SCHEMATIC DIAGRAM.


P901
R952
1K
1
TO SWITCH S6
C923
4700
R950
15K
R951
15K
C922
680
CR924
G-46
R953
10K
CR923
12 TO CARD E-9
11 TO -12V
R946
30K
10 TO CARDS D-17, A-13, H-22
C920
680
C921
680
G-9
CR922
5 TO CARD B-11
R945
10K
R947
10K
9 TO GROUND
925
8 +6V
R943
39K
R948
56K
R949
56K
6
TO CARDS B-9, A-12
7
TO CARDS H-4, H-20, G-7

R (CARD I), SCHEMATIC DIAGRAM.


FF-34
FF-35
FF-36
FF-37
FF-38
P901
R952 1K
① TO SWITCH S6
C923 4700
R950 15K
R951 15K
C922 680
CR924
R953 10K
G-46
CR923
⑫ TO CARD E-9
⑪ TO -12V
⑩ TO CARDS D-17, A-13, H-22
⑤ TO CARD B-11
⑨ TO GROUND
⑧ +6V
R901 2.4K
R902 2.4K
C901 270
C902 270
C903 150
R903 39K
R904 39K
R905 30K
R906 30K
C904 150
CR 903
CR 904
Q901
Q902
CR 902
CR 901
R907 39K
R908 39K
R909 2.4K
R910 2.4K
C905 270
C906 270
C907 150
R911 39K
R912 39K
R913 30K
R914 30K
C908 150
CR906
CR907
Q903
Q904
CR 905
CR 908
R915 39K
R916 39K
R917 2.4K
R918 2.4K
C927 270
C909 270
C910 150
R919 39K
R920 39K
R921 30K
R922 30K
C911 150
CR910
CR911
Q905
Q906
CR 909
CR 912
R923 39K
R924 39K
R925 2.4K
R926 2.4K
C912 270
C913 270
C926 150
R927 39K
R928 39K
R929 30K
R930 30K
C914 150
CR914
CR915
Q907
Q908
CR 913
CR 916
R932 39K
R933 39K
CR 917
R934 2.4K
R935 2.4K
C917 150
R936 30K
R937 30K
C918 150
Q909
Q910
CR926
R944 30K
R946 30K
G-12
G-9
C920 680
C921 680
CR921
CR922
R945 10K
R947 10K
R939 39K
R938 39K
CR918
CR919
CR920
CR925
C915 270
R940 39K
C916 270
R941 39K
C919 270
R942 39K
C926 270
R943 39K
R948 56K
R949 56K
C924 4700
C925 4700
SPEED CHANGER JUMPER
60 WPM
100 WPM
60 WPM
100 WPM
② TO RELAY K11-C
ON
OFF
AUTOMATIC SPECIAL CHARACTER
③ TO CARD G-10
④ TO CARD G-11
⑥ TO CARDS B-9, A-12
⑦ TO CARDS H-4, H-20, G-7

NOTES:

1. UNLESS OTHERWISE NOTED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN UUF.

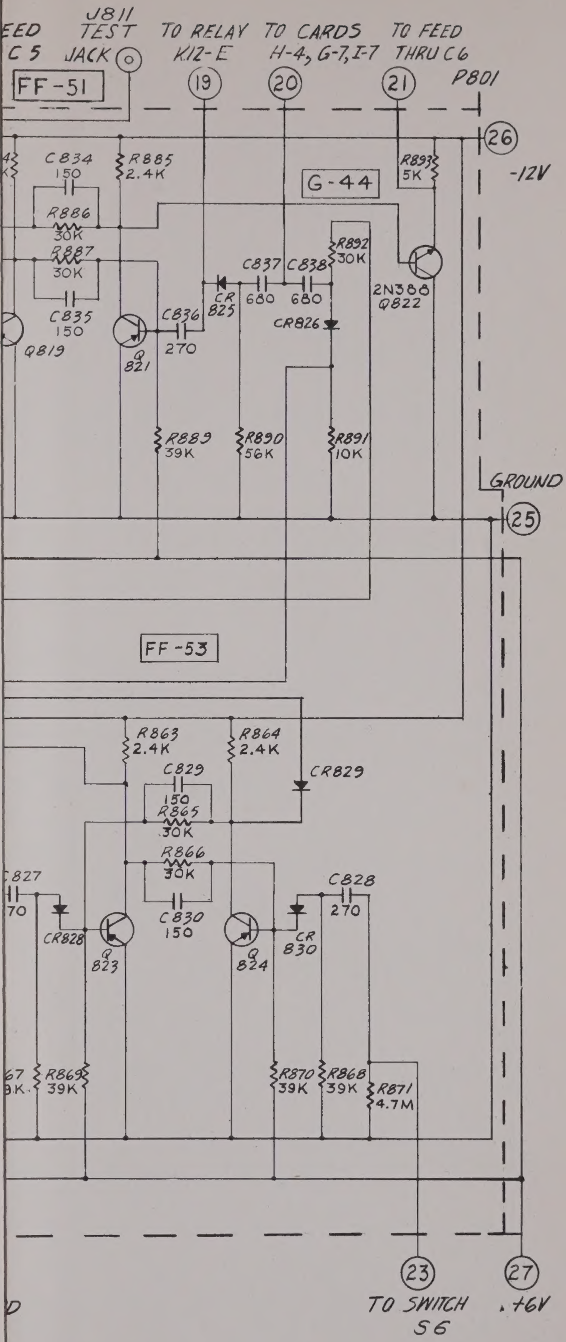
   TRANSISTORS: 2N404

   DIODES: IN198

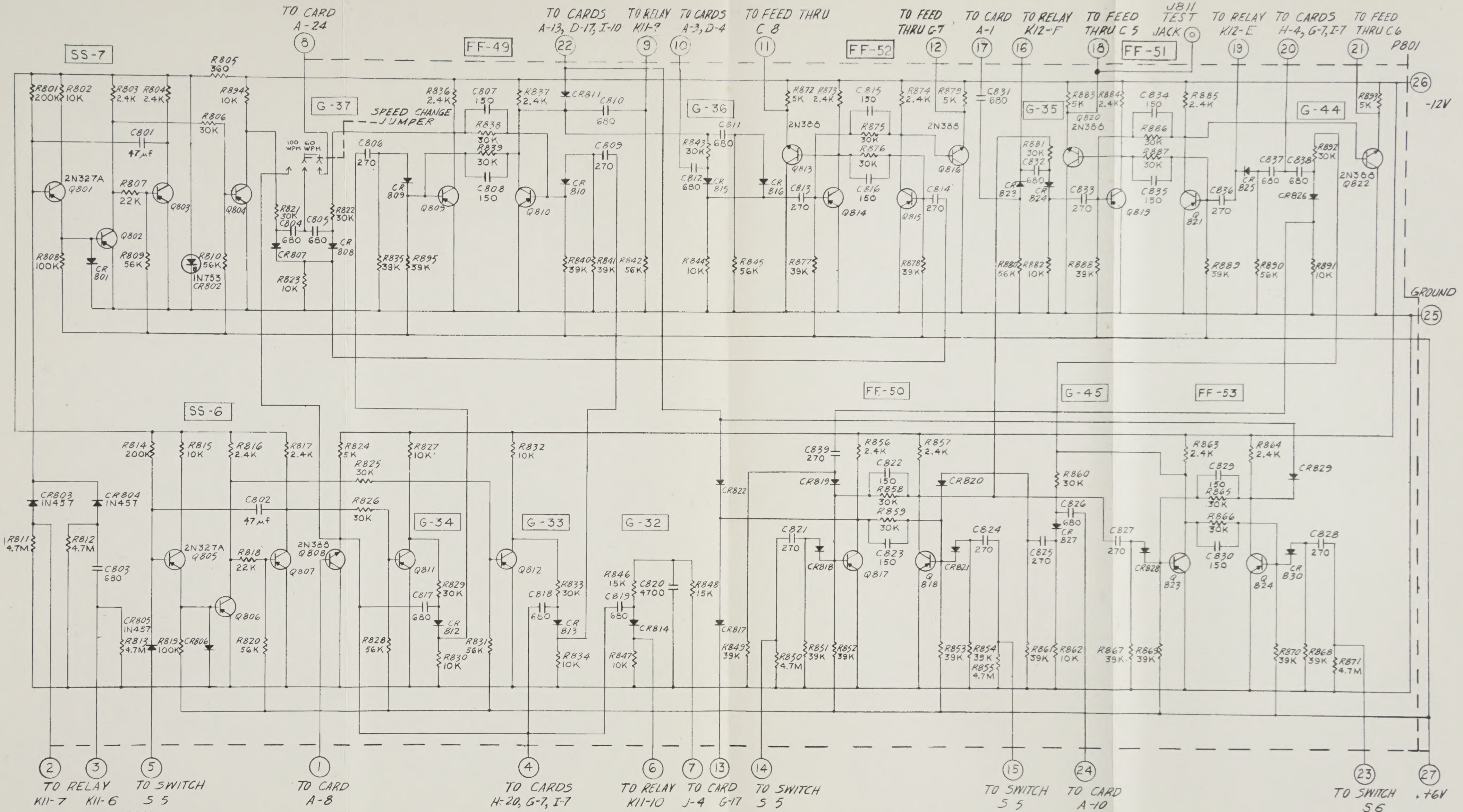
2. ⑤ INDICATES CONNECTOR PIN.

3. LETTER AND NUMBER COMBINATION INDICATES CARD AND PIN.

FIG.11. DELAY CORRECTOR (CARD I), SCHEMATIC DIAGRAM.


EED
C 5
J811
TEST
JACK
TO RELAY
K12-E
TO CARDS
H-4, G-7, I-7
TO FEED
THRU C6
P801
FF-51
19
20
21
26
-12V
C834
150
R885
2.4K
G-44
R893
5K
R886
30K
R887
30K
R892
30K
C837
C838
680
680
CR
825
2N388
Q822
C835
150
C836
270
CR826
Q819
Q
821
R889
39K
R890
56K
R891
10K
GROUND
25
FF-53
R863
2.4K
R864
2.4K
CR829
C829
150
R865
30K
R866
30K
C827
70
C828
270
CR828
Q
823
C830
150
Q
824
CR
830
67
9K
R869
39K
R870
39K
R868
39K
R871
4.7M
23
27
D
TO SWITCH
S6
+6V

(CARD H), SCHEMATIC DIAGRAM.


TO CARD A-24
TO CARDS A-13, D-17, I-10
TO RELAY K11-9
TO CARDS A-3, D-4
TO FEED THRU C 8
TO FEED THRU G-7
TO CARD A-1
TO RELAY K12-F
TO FEED THRU C 5
J811 TEST JACK
TO RELAY K12-E
TO CARDS H-4, G-7, I-7
TO FEED THRU C6
P801
-12V
GROUND
SS-7
FF-49
G-37
SPEED CHANGE JUMPER
100 WPM
60 WPM
G-36
FF-52
G-35
FF-51
G-44
SS-6
G-34
G-33
G-32
FF-50
G-45
FF-53
2N327A Q801
2N327A Q805
2N388 Q808
2N388 Q820
2N388 Q822
1N753 CR802
CR803 1N457
CR804 1N457
CR805 1N457
C801 47μf
C802 47μf
C820 4700
TO RELAY K11-7
TO RELAY K11-6
TO SWITCH S 5
TO CARD A-8
TO CARDS H-20, G-7, I-7
TO RELAY K11-10
TO CARD J-4
TO CARD G-17
TO SWITCH S 5
TO SWITCH S 5
TO CARD A-10
TO SWITCH S6
+6V

NOTES:

1. UNLESS OTHERWISE NOTED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN UUF.

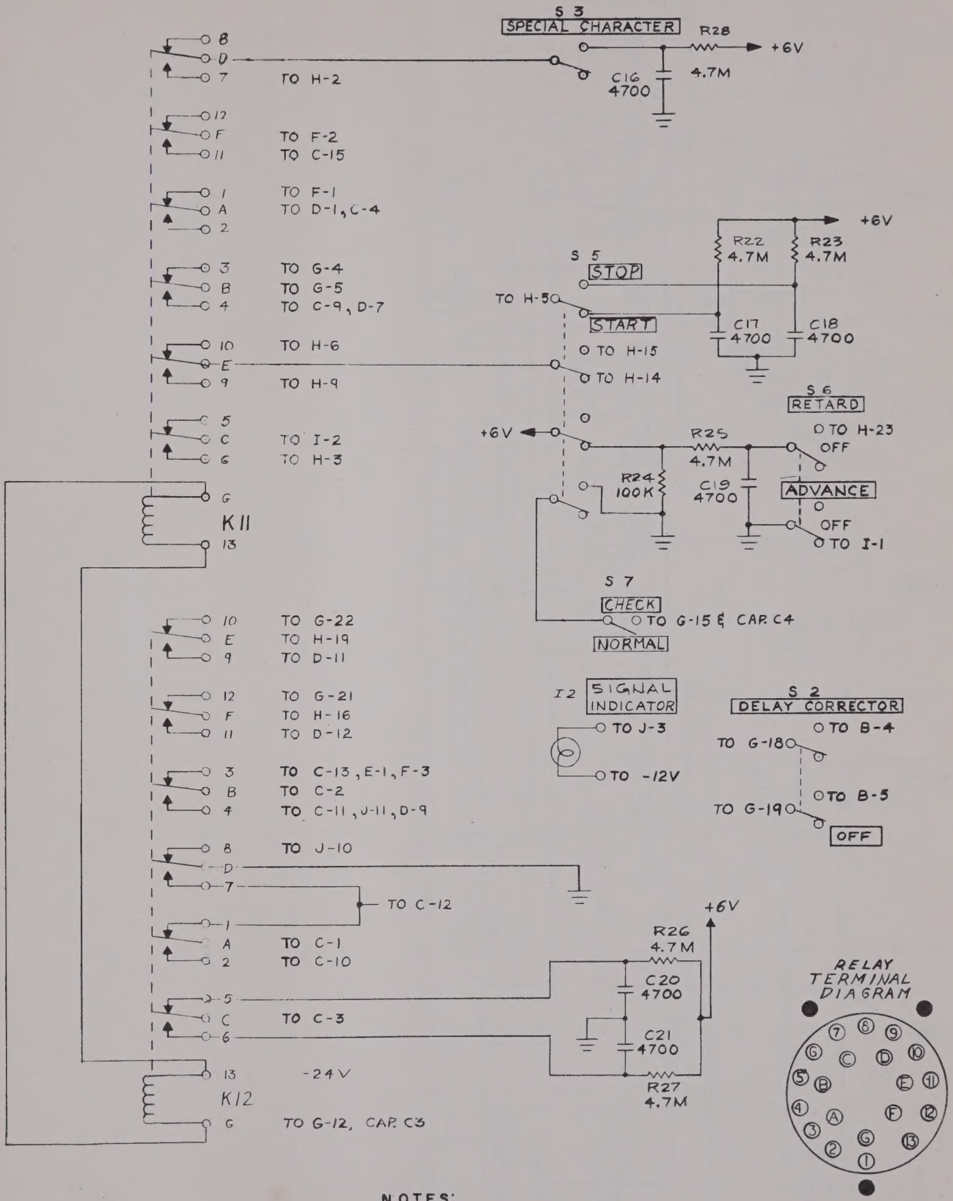
TRANSISTORS: 2N404

DIODES: IN198

2. ⑤ INDICATES CONNECTOR PIN.

3. LETTER AND NUMBER COMBINATION INDICATES CARD AND PIN.

FIG. 12. START-STOP (CARD H), SCHEMATIC DIAGRAM.

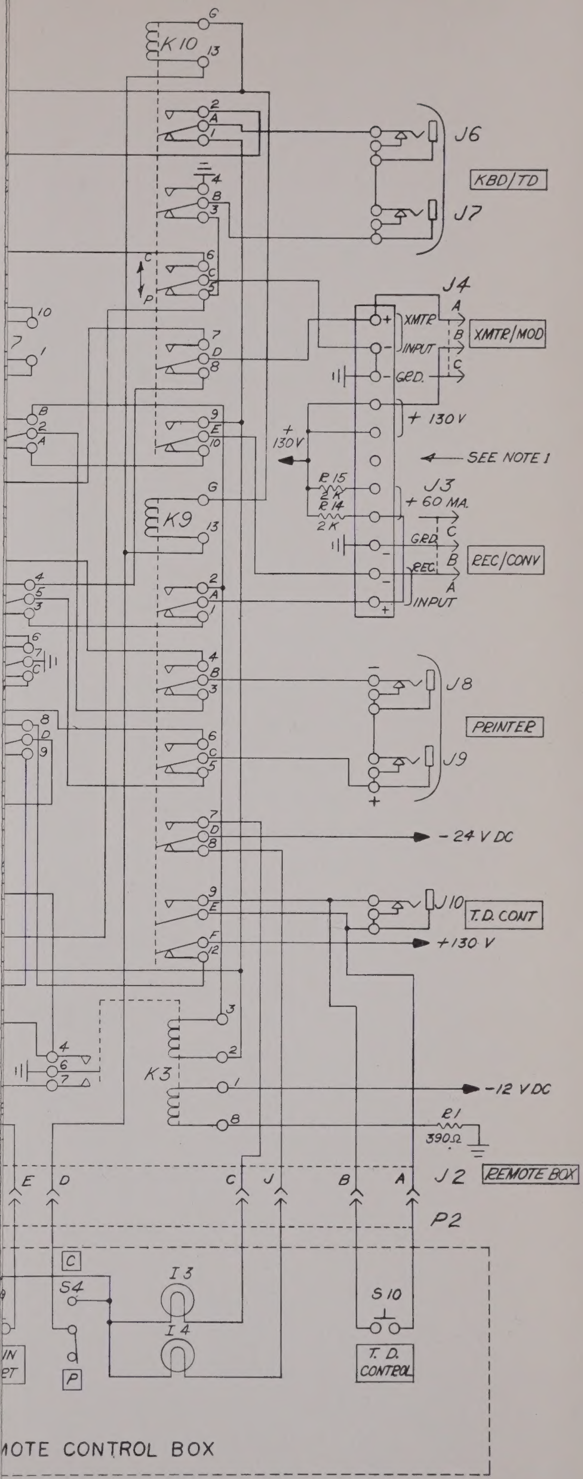

S 3
SPECIAL CHARACTER
R28
+6V
4.7M
C16
4700
8
D
7
TO H-2
12
F
11
TO F-2
TO C-15
1
A
2
TO F-1
TO D-1, C-4
3
B
4
TO G-4
TO G-5
TO C-9, D-7
10
E
9
TO H-6
TO H-9
5
C
6
TO I-2
TO H-3
G
K11
13
+6V
R22
4.7M
R23
4.7M
S 5
STOP
TO H-5
START
C17
4700
C18
4700
TO H-15
TO H-14
S 6
RETARD
TO H-23
OFF
+6V
R25
4.7M
R24
100K
C19
4700
ADVANCE
OFF
TO I-1
S 7
CHECK
TO G-15 & CAR C4
NORMAL
I2
SIGNAL INDICATOR
TO J-3
TO -12V
S 2
DELAY CORRECTOR
TO G-18
TO B-4
TO G-19
TO B-5
OFF
10
E
9
TO G-22
TO H-19
TO D-11
12
F
11
TO G-21
TO H-16
TO D-12
3
B
4
TO C-13, E-1, F-3
TO C-2
TO C-11, J-11, D-9
8
D
7
TO J-10
TO C-12
1
A
2
TO C-1
TO C-10
+6V
R26
4.7M
C20
4700
5
C
6
TO C-3
C21
4700
R27
4.7M
13
-24V
K12
G
TO G-12, CAR C3
RELAY TERMINAL DIAGRAM
⑦ ⑧ ⑨
⑥ Ⓒ Ⓓ ⑩
⑤ Ⓑ Ⓔ ⑪
④ Ⓐ Ⓕ ⑫
③ ② Ⓖ ⑬
①

NOTES:

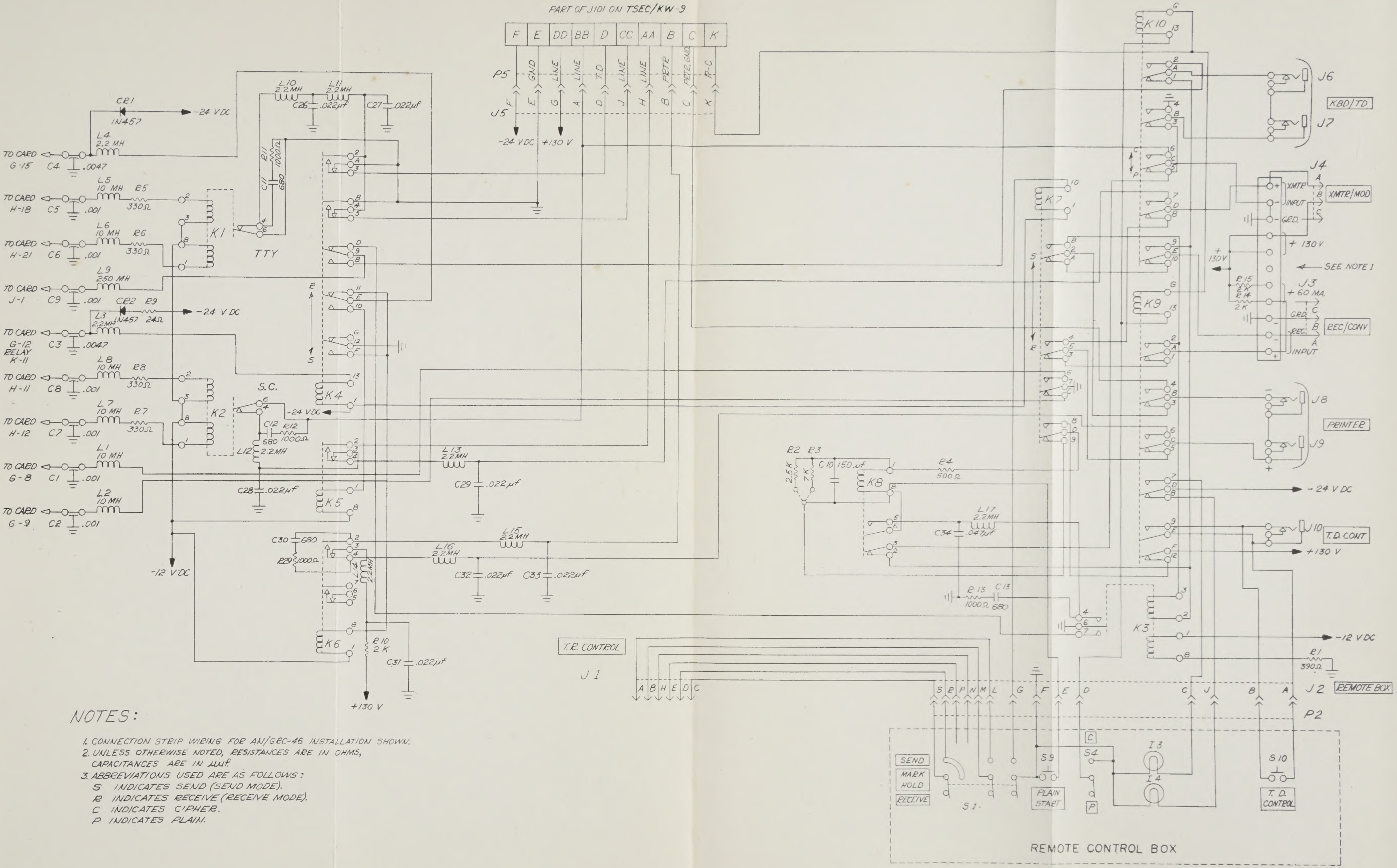
1. UNLESS OTHERWISE NOTED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN UUF.

2. LETTER AND NUMBER COMBINATION INDICATES CARD AND PIN

FIG. 13. LOGIC CIRCUIT SWITCHES AND RELAYS.


K10
G
13
2
A
1
4
B
3
6
C
5
P
7
D
8
9
E
10
J6
KBD/TD
J7
J4
XMTR
INPUT
GRD.
A
B
C
XMTR/MOD
+ 130 V
+
130V
SEE NOTE 1
R15
2K
R14
2K
J3
+ 60 MA.
GRD.
REC.
INPUT
REC/CONV
K9
G
13
J8
PRINTER
J9
- 24 V DC
J10
T.D. CONT
+130 V
F
12
K3
-12 VDC
R1
390Ω
J2
REMOTE BOX
E
D
C
J
B
A
P2
C
S4
I3
I4
P
S10
T. D.
CONTROL
IN
ET
MOTE CONTROL BOX

RELAYS, SCHEMATIC DIAGRAM.


PART OF J101 ON TSEC/KW-9
F E DD BB D CC AA B C K
P5
GND LINE LINE T.D. LINE LINE PETR PETR. GND. P-C
J5
F E G A D J H B C K
-24 VDC +130 V
TO CARD G-15 C4 .0047
CR1 1N457 -24 V DC
L4 2.2 MH
TO CARD H-18 C5 .001 L5 10 MH R5 330Ω
TO CARD H-21 C6 .001 L6 10 MH R6 330Ω
TO CARD J-1 C9 .001 L9 250 MH
CR2 1N457 R9 24Ω -24 V DC
TO CARD G-12 RELAY K-11 C3 .0047 L3 2.2MH
TO CARD H-11 C8 .001 L8 10 MH R8 330Ω
TO CARD H-12 C7 .001 L7 10 MH R7 330Ω
TO CARD G-8 C1 .001 L1 10 MH
TO CARD G-9 C2 .001 L2 10 MH
-12 V DC
K1 TTY
K2 S.C.
L10 2.2 MH L11 2.2 MH C26 .022µf C27 .022µf
R11 1000Ω C11 680
C12 680 R12 1000Ω L12 2.2MH
-24 VDC
C28 .022µf
K4 K5 K6
L13 2.2MH C29 .022µf
C30 680 R29 1000Ω L14 2.2MH
L15 2.2MH L16 2.2MH C32 .022µf C33 .022µf
R10 2K C31 .022µf
+130 V
R S
K10 K7 K9 K8 K3
C P
R2 R3 2.5K 7K C10 150µf R4 500Ω
L17 2.2MH C34 .047µf
R13 1000Ω C13 680
J6 J7 KBD/TD
J4 XMTR INPUT GRD. A B C XMTR/MOD
+ 130V 130V SEE NOTE 1
R15 2K R14 2K J3 + 60 MA.
GRD. REC. INPUT C B A REC/CONV
J8 J9 PRINTER
-24 V DC
J10 T.D. CONT +130 V
-12 V DC
R1 390Ω
T.R. CONTROL J1
A B H E D C
S R P N M L G F E D C J B A
J2 REMOTE BOX P2
SEND MARK HOLD RECEIVE S1
S9 PLAIN START
C S4 P
I3 I4
S10 T.D. CONTROL
REMOTE CONTROL BOX

NOTES:

1. CONNECTION STRIP WIRING FOR AN/GRC-46 INSTALLATION SHOWN.
2. UNLESS OTHERWISE NOTED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN µµf.
3. ABBREVIATIONS USED ARE AS FOLLOWS:
   - S INDICATES SEND (SEND MODE).
   - R INDICATES RECEIVE (RECEIVE MODE).
   - C INDICATES CIPHER.
   - P INDICATES PLAIN.

FIG. 14, INPUT-OUTPUT RELAYS, SCHEMATIC DIAGRAM.

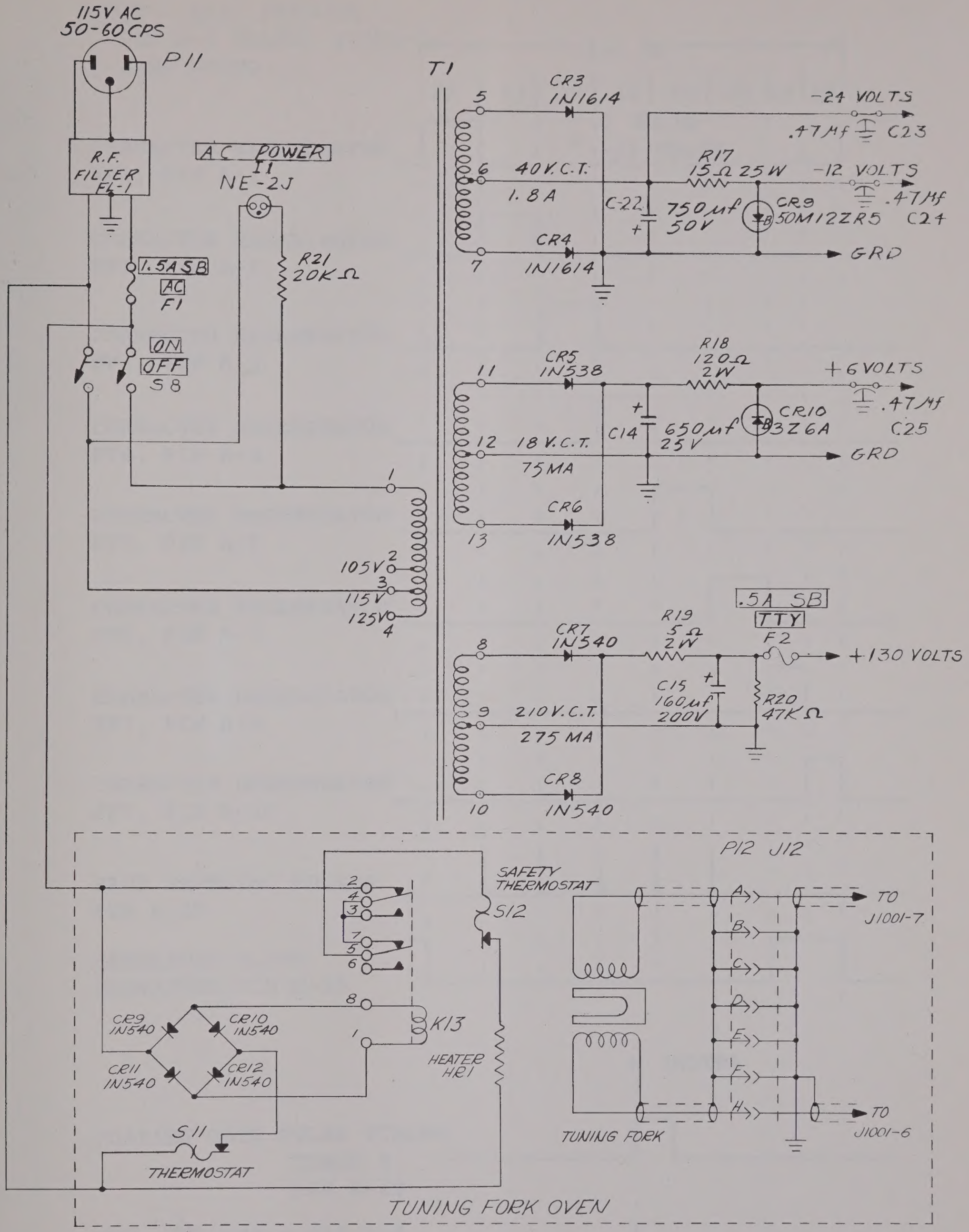
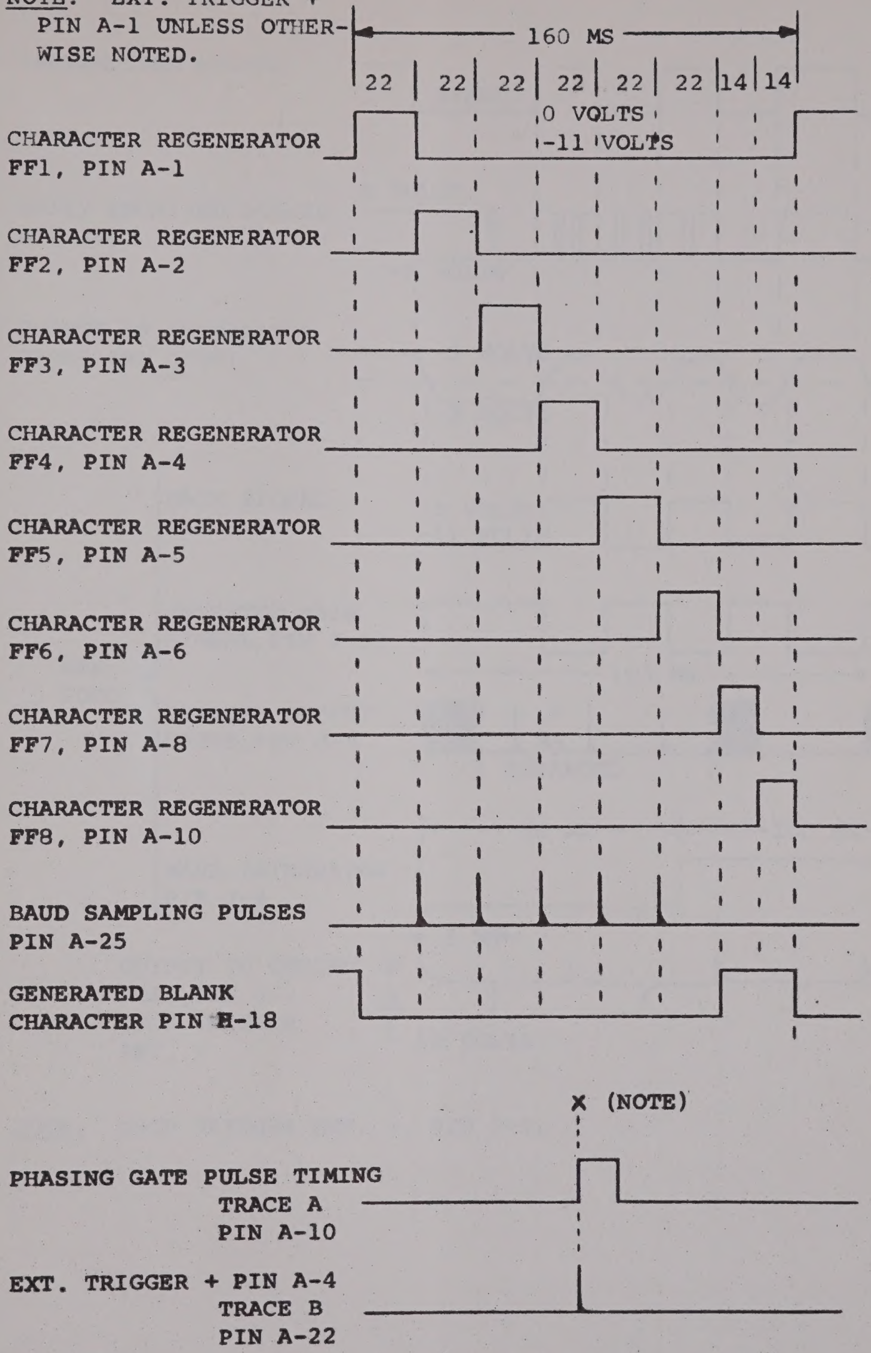

115V AC
50-60 CPS
P11
R.F. FILTER FL-1
AC POWER
I1
NE-2J
R21
20KΩ
1.5A SB
AC
F1
ON
OFF
S8
T1
5
CR3
1N1614
-24 VOLTS
.47Mf
C23
6
40V.C.T.
1.8A
R17
15Ω 25W
-12 VOLTS
.47Mf
C24
C-22
750μf
50V
CR9
50M12ZR5
7
CR4
1N1614
GRD
11
CR5
1N538
R18
120Ω
2W
+6 VOLTS
.47Mf
C25
C14
650μf
25V
CR10
3Z6A
12
18V.C.T.
75MA
GRD
13
CR6
1N538
1
2
105V
3
115V
125V
4
.5A SB
TTY
F2
8
CR7
1N540
R19
5Ω
2W
+130 VOLTS
C15
160μf
200V
R20
47KΩ
9
210V.C.T.
275 MA
10
CR8
1N540
P12 J12
SAFETY THERMOSTAT
S12
2
4
3
7
5
6
8
1
K13
A
B
C
D
E
F
H
TO J1001-7
TO J1001-6
CR9 1N540
CR10 1N540
CR11 1N540
CR12 1N540
HEATER HR1
S11
THERMOSTAT
TUNING FORK
TUNING FORK OVEN

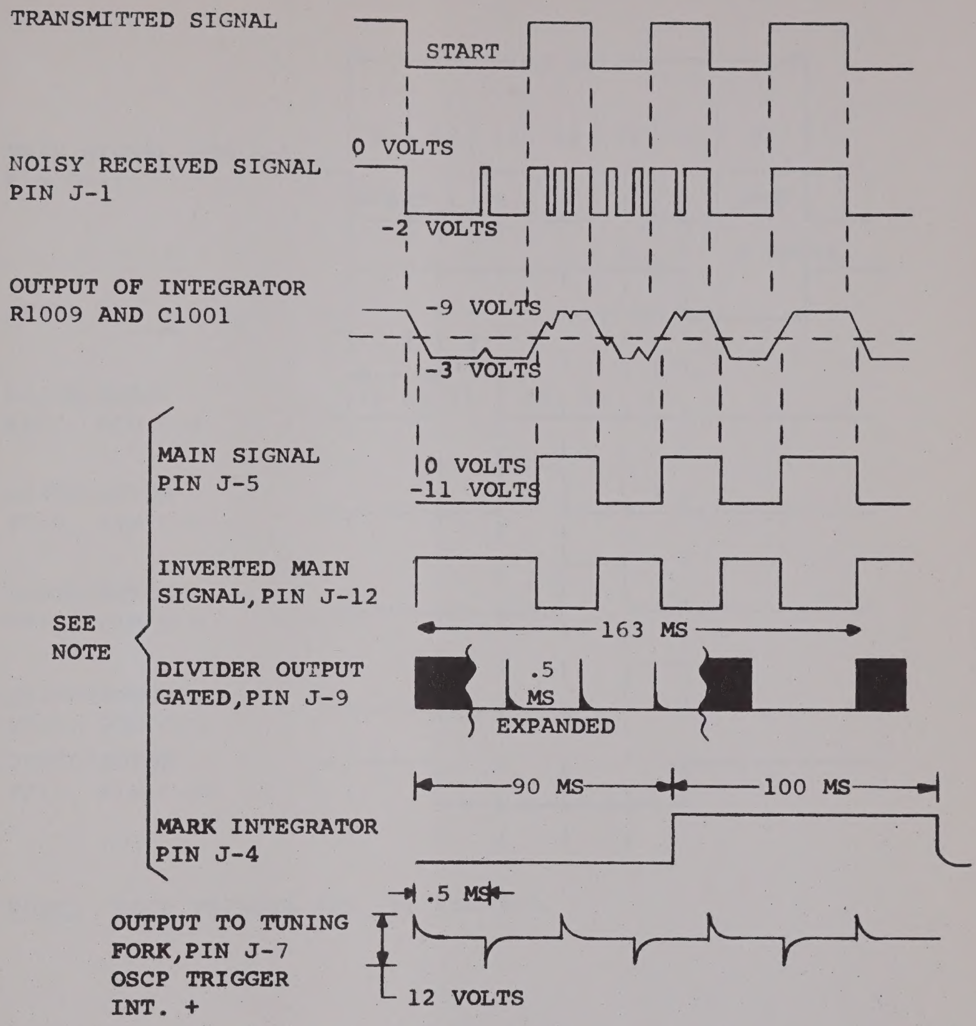
FIG. 15. POWER SUPPLY AND TUNING FORK OVEN, SCHEMATIC DIAGRAM.

NOTE: EXT. TRIGGER + PIN A-1 UNLESS OTHERWISE NOTED.


160 MS
22
22
22
22
22
22
14
14
0 VOLTS
-11 VOLTS
CHARACTER REGENERATOR FF1, PIN A-1
CHARACTER REGENERATOR FF2, PIN A-2
CHARACTER REGENERATOR FF3, PIN A-3
CHARACTER REGENERATOR FF4, PIN A-4
CHARACTER REGENERATOR FF5, PIN A-5
CHARACTER REGENERATOR FF6, PIN A-6
CHARACTER REGENERATOR FF7, PIN A-8
CHARACTER REGENERATOR FF8, PIN A-10
BAUD SAMPLING PULSES PIN A-25
GENERATED BLANK CHARACTER PIN H-18
X (NOTE)
PHASING GATE PULSE TIMING
TRACE A
PIN A-10
EXT. TRIGGER + PIN A-4
TRACE B
PIN A-22

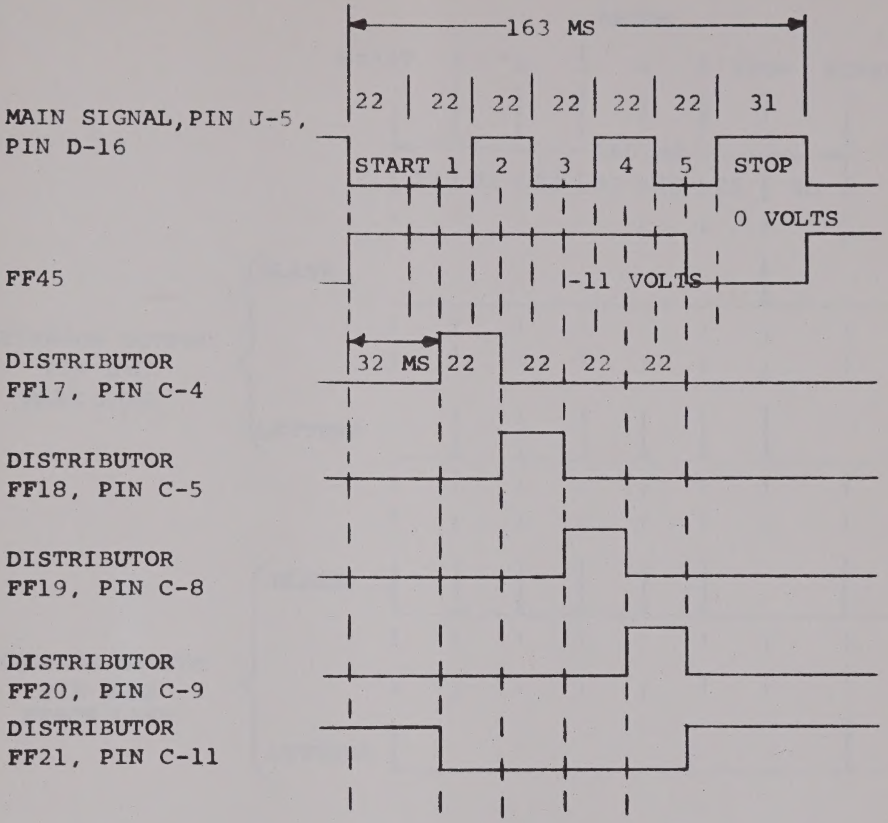
NOTE: X MARKS CORRECT PHASING POINT.

FIG. 16. CHARACTER REGENERATOR TIMING (CARD A).


TRANSMITTED SIGNAL
START
0 VOLTS
NOISY RECEIVED SIGNAL PIN J-1
-2 VOLTS
OUTPUT OF INTEGRATOR R1009 AND C1001
-9 VOLTS
-3 VOLTS
MAIN SIGNAL PIN J-5
0 VOLTS
-11 VOLTS
INVERTED MAIN SIGNAL, PIN J-12
163 MS
SEE NOTE
DIVIDER OUTPUT GATED, PIN J-9
.5 MS
EXPANDED
90 MS
100 MS
MARK INTEGRATOR PIN J-4
.5 MS
OUTPUT TO TUNING FORK, PIN J-7
OSCP TRIGGER INT. +
12 VOLTS

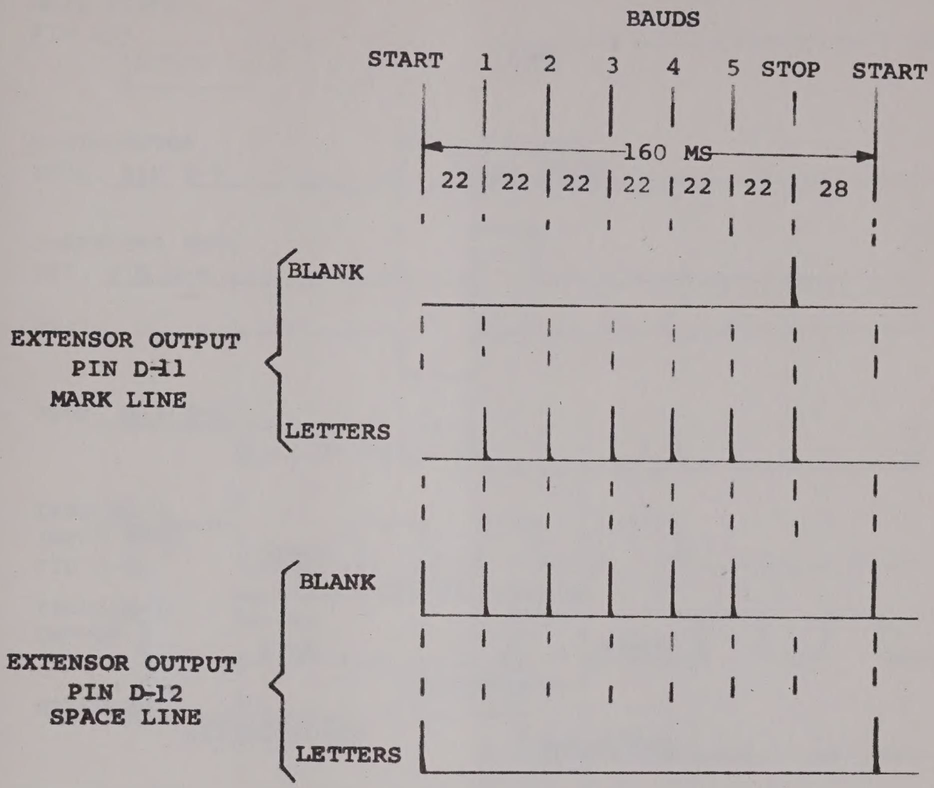
NOTE: OSCP TRIGGER EXT. -, PIN J-5.

FIG. 17. MAIN SIGNAL INTEGRATOR TIMING (CARD J).


163 MS
22
22
22
22
22
22
31
MAIN SIGNAL, PIN J-5, PIN D-16
START
1
2
3
4
5
STOP
0 VOLTS
FF45
-11 VOLTS
DISTRIBUTOR FF17, PIN C-4
32 MS
22
22
22
22
DISTRIBUTOR FF18, PIN C-5
DISTRIBUTOR FF19, PIN C-8
DISTRIBUTOR FF20, PIN C-9
DISTRIBUTOR FF21, PIN C-11

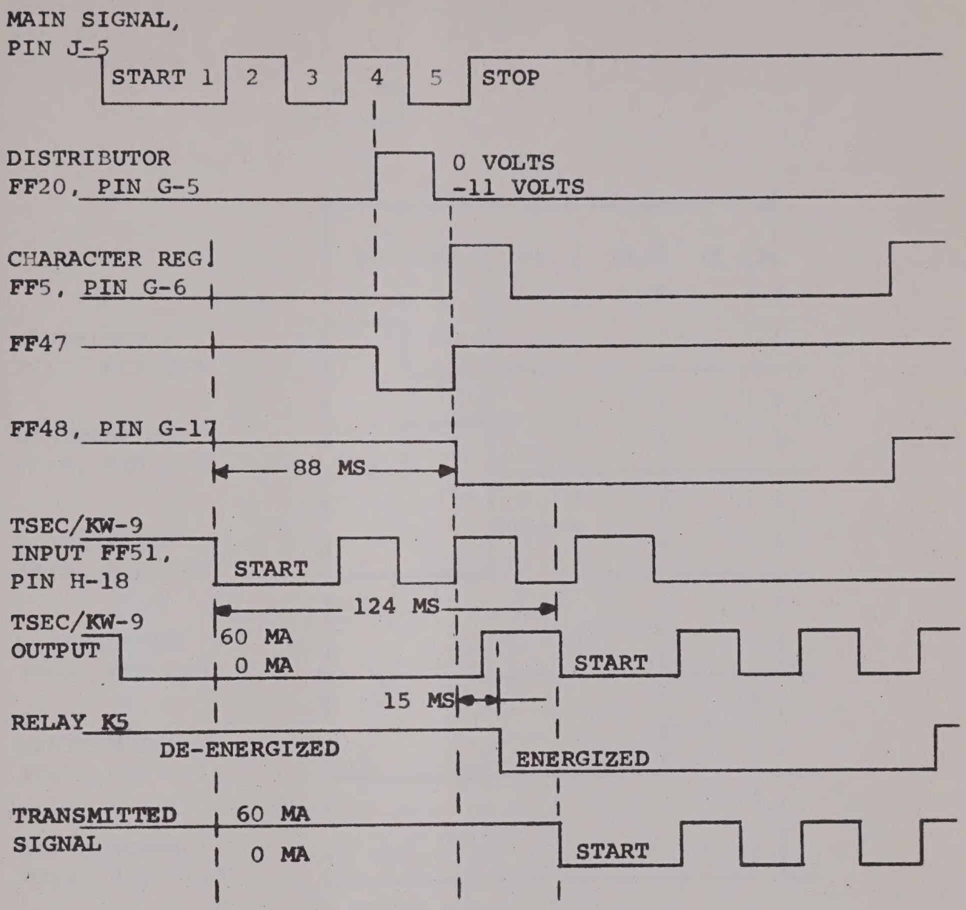
NOTE: OSCP TRIGGER EXT. +, PIN J-5.

FIG. 18. DISTRIBUTOR TIMING (CARD C) SEND MODE.


BAUDS
START
1
2
3
4
5
STOP
START
160 MS
22
22
22
22
22
22
28
BLANK
EXTENSOR OUTPUT
PIN D-11
MARK LINE
LETTERS
BLANK
EXTENSOR OUTPUT
PIN D-12
SPACE LINE
LETTERS

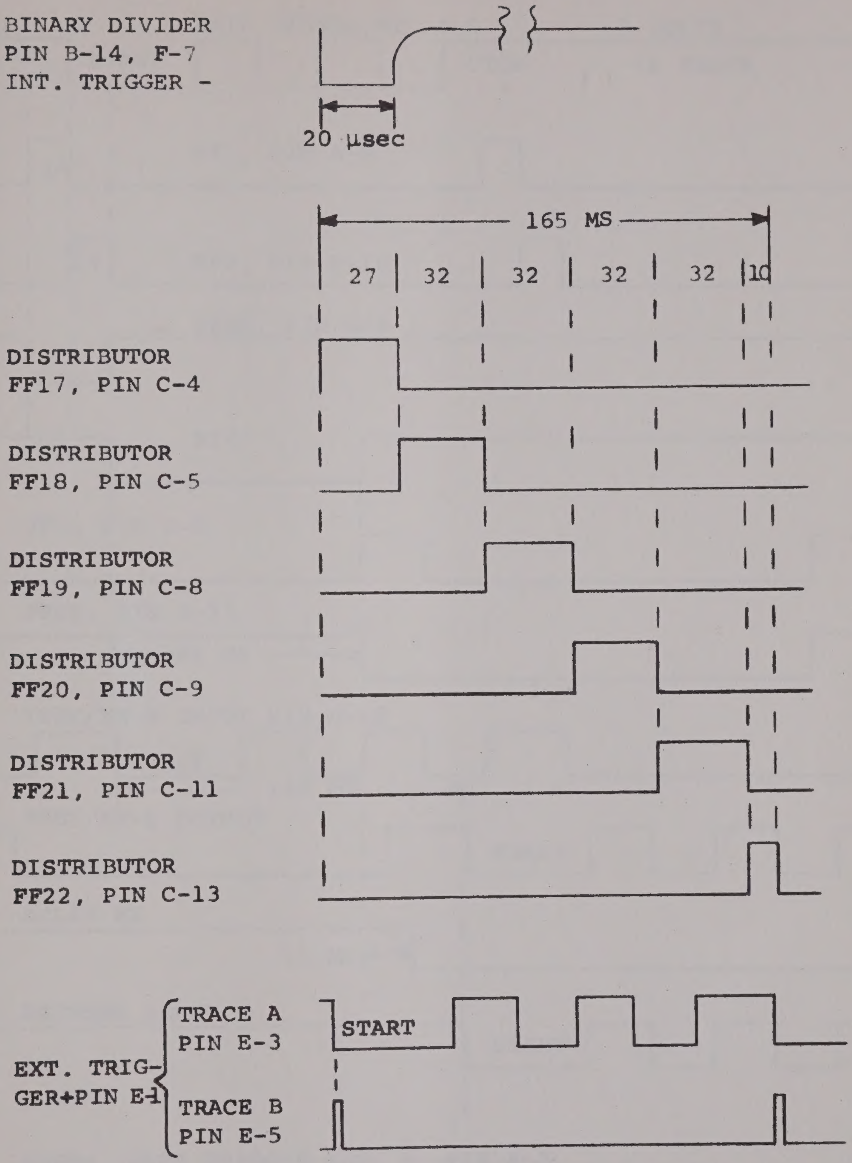
NOTE: OSCP TRIGGER EXT. +, PIN A-1.

FIG. 19. EXTENSOR OUTPUT TIMING (CARD D).


MAIN SIGNAL,
PIN J-5
START 1
2
3
4
5
STOP
DISTRIBUTOR
FF20, PIN G-5
0 VOLTS
-11 VOLTS
CHARACTER REG
FF5, PIN G-6
FF47
FF48, PIN G-17
88 MS
TSEC/KW-9
INPUT FF51,
PIN H-18
START
124 MS
TSEC/KW-9
OUTPUT
60 MA
0 MA
START
15 MS
RELAY K5
DE-ENERGIZED
ENERGIZED
TRANSMITTED
SIGNAL
60 MA
0 MA
START

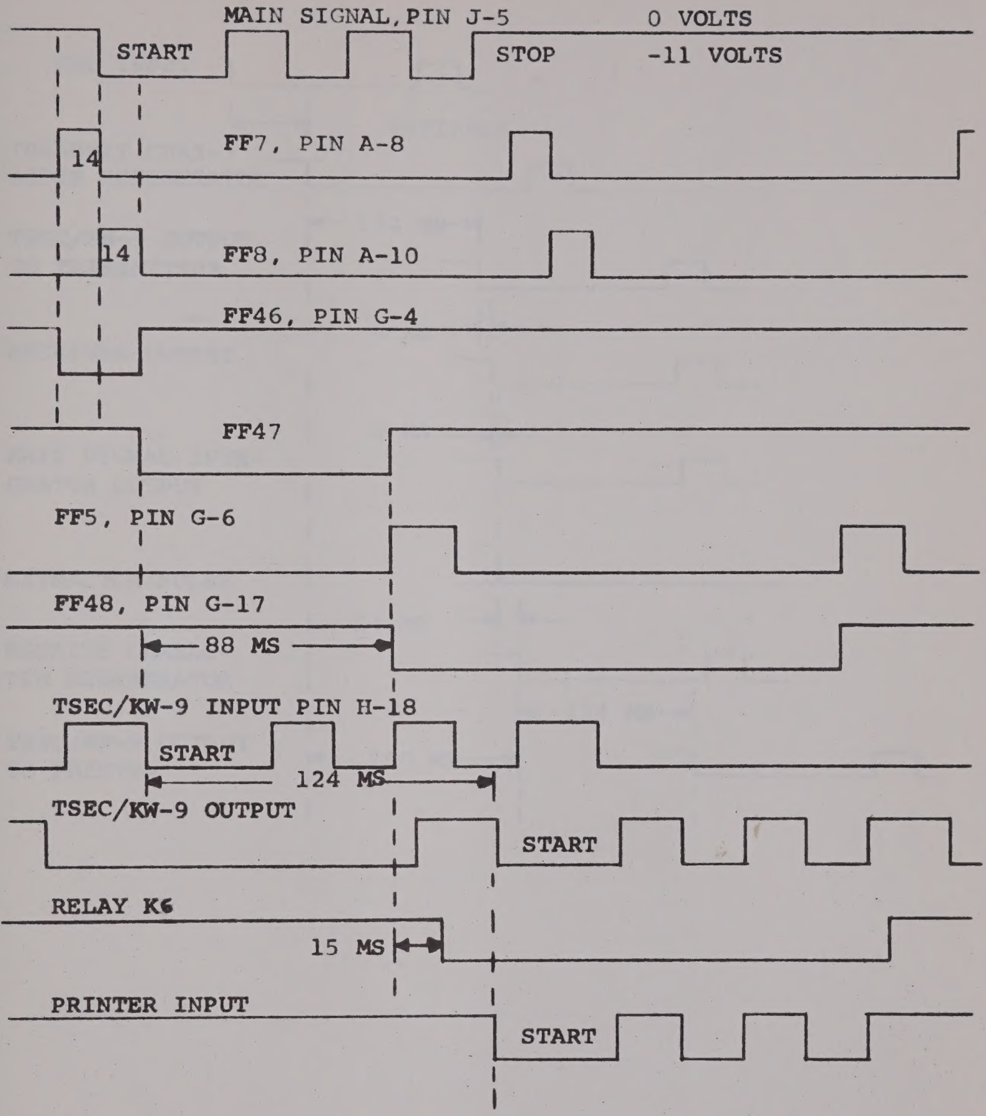
NOTE: OSCP TRIGGER EXT. -, PIN J-5

FIG. 20. OUTPUT CONTROL TIMING (CARD G)
SEND MODE.


BINARY DIVIDER
PIN B-14, F-7
INT. TRIGGER -
20 µsec
165 MS
27
32
32
32
32
10
DISTRIBUTOR
FF17, PIN C-4
DISTRIBUTOR
FF18, PIN C-5
DISTRIBUTOR
FF19, PIN C-8
DISTRIBUTOR
FF20, PIN C-9
DISTRIBUTOR
FF21, PIN C-11
DISTRIBUTOR
FF22, PIN C-13
EXT. TRIGGER+PIN E-1
TRACE A
PIN E-3
START
TRACE B
PIN E-5

NOTE: OSCP TRIGGER EXT. +, PIN C-4 UNLESS OTHERWISE INDICATED.

FIG. 21. DISTRIBUTOR (CARD C) AND EXTRACTOR (CARD E) TIMING.


MAIN SIGNAL, PIN J-5
0 VOLTS
START
STOP
-11 VOLTS
14
FF7, PIN A-8
14
FF8, PIN A-10
FF46, PIN G-4
FF47
FF5, PIN G-6
FF48, PIN G-17
88 MS
TSEC/KW-9 INPUT PIN H-18
START
124 MS
TSEC/KW-9 OUTPUT
START
RELAY K6
15 MS
PRINTER INPUT
START

NOTE: OSCP TRIGGER EXT. +, PIN A-8.

FIG. 22. OUTPUT CONTROL TIMING (CARD G) RECEIVE MODE.

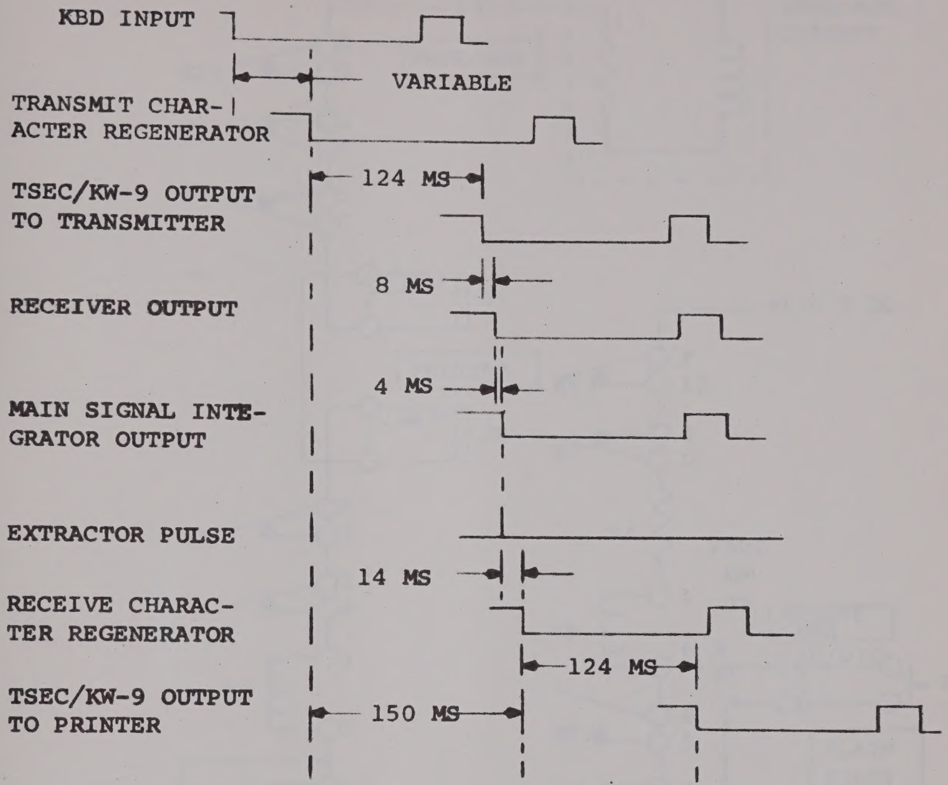
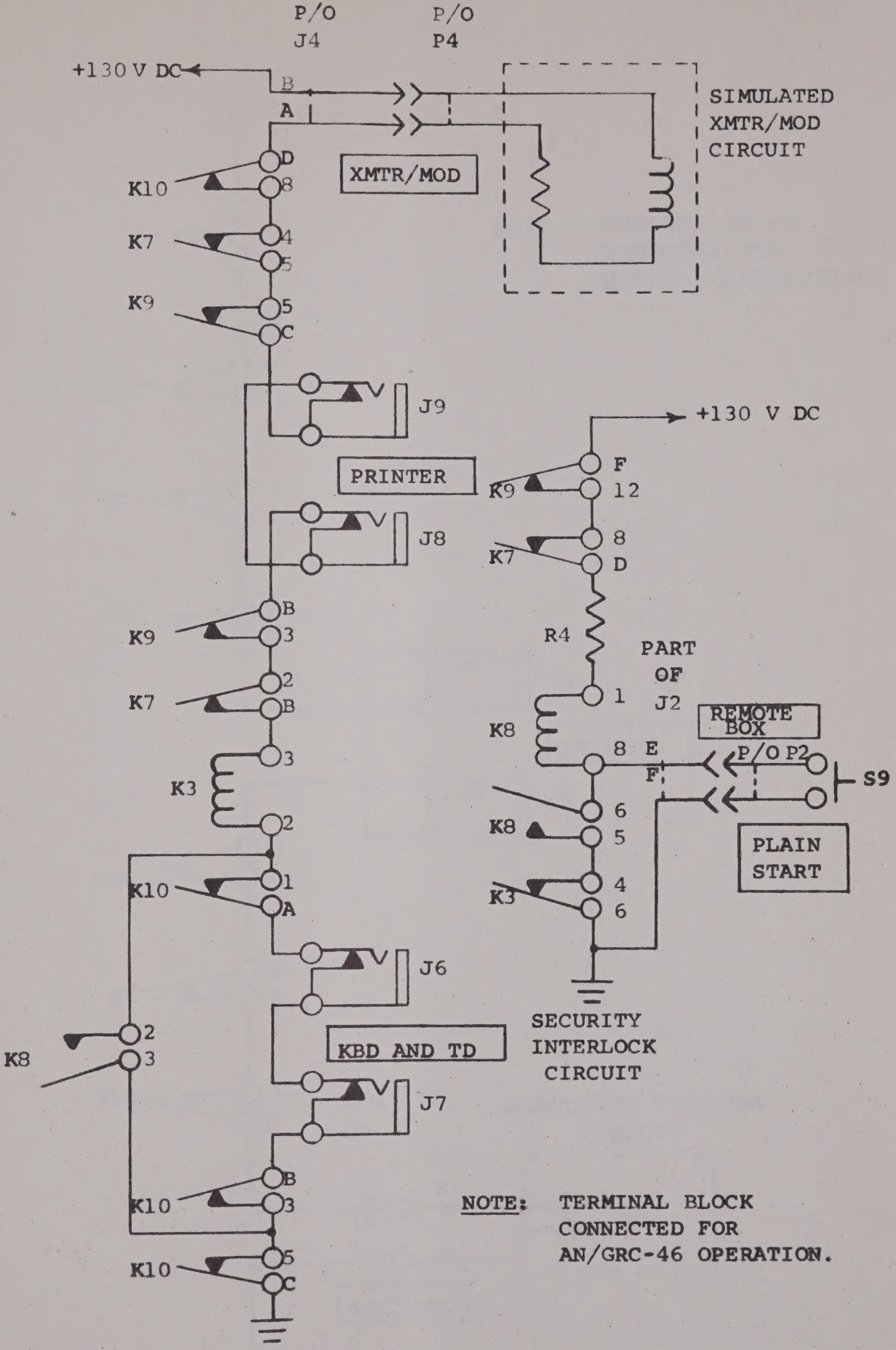

KBD INPUT
VARIABLE
TRANSMIT CHARACTER REGENERATOR
124 MS
TSEC/KW-9 OUTPUT TO TRANSMITTER
8 MS
RECEIVER OUTPUT
4 MS
MAIN SIGNAL INTEGRATOR OUTPUT
EXTRACTOR PULSE
14 MS
RECEIVE CHARACTER REGENERATOR
124 MS
TSEC/KW-9 OUTPUT TO PRINTER
150 MS

FIG. 23. SYNCHRONIZER PHASE TIMING.


P/O
J4
P/O
P4
+130 V DC
B
A
SIMULATED
XMTR/MOD
CIRCUIT
XMTR/MOD
K10
D
8
K7
4
5
K9
5
C
J9
PRINTER
+130 V DC
F
K9
12
J8
K7
8
D
B
K9
3
R4
PART
OF
J2
2
K7
B
1
K8
3
REMOTE
BOX
K3
8
E
P/O P2
F
S9
6
K8
5
2
PLAIN
START
K10
1
A
4
K3
6
J6
SECURITY
INTERLOCK
CIRCUIT
2
K8
3
KBD AND TD
J7
B
K10
3
K10
5
C

NOTE: TERMINAL BLOCK CONNECTED FOR AN/GRC-46 OPERATION.

FIG. 24. SIMPLIFIED RELAY CIRCUIT, PLAIN SEND.

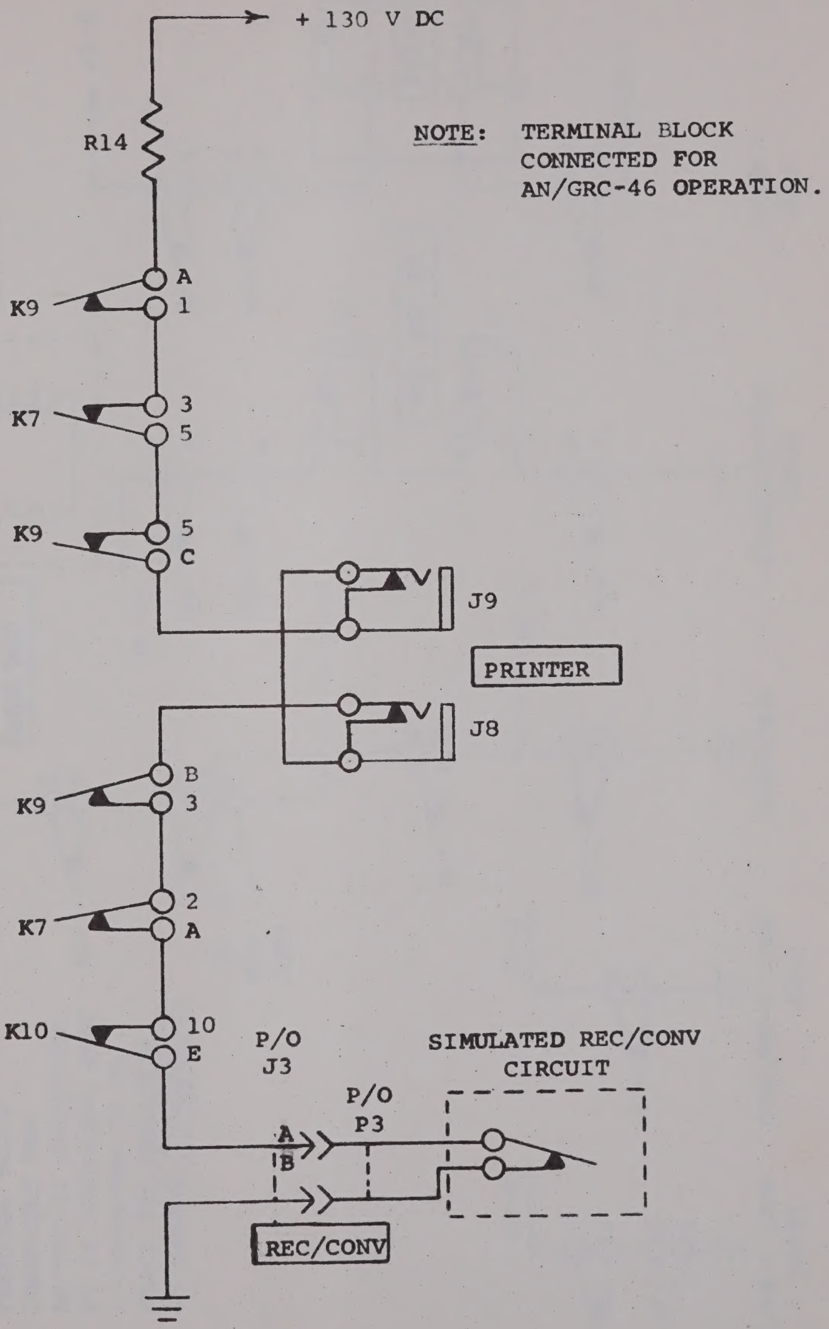
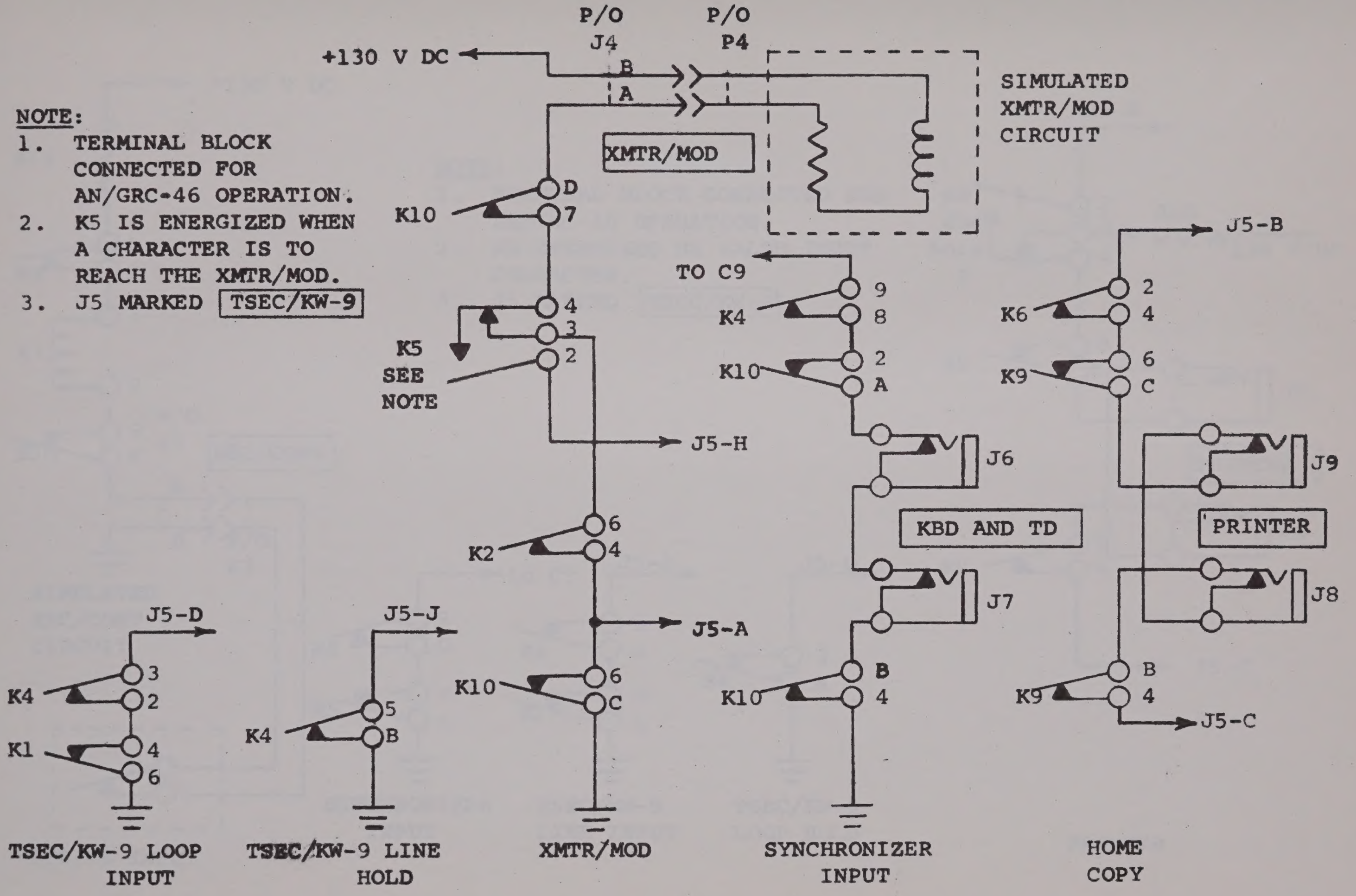

+ 130 V DC
R14
NOTE: TERMINAL BLOCK CONNECTED FOR AN/GRC-46 OPERATION.
K9
A
1
K7
3
5
K9
5
C
J9
PRINTER
J8
B
K9
3
K7
2
A
K10
10
E
P/O
J3
SIMULATED REC/CONV
CIRCUIT
P/O
P3
A
B
REC/CONV

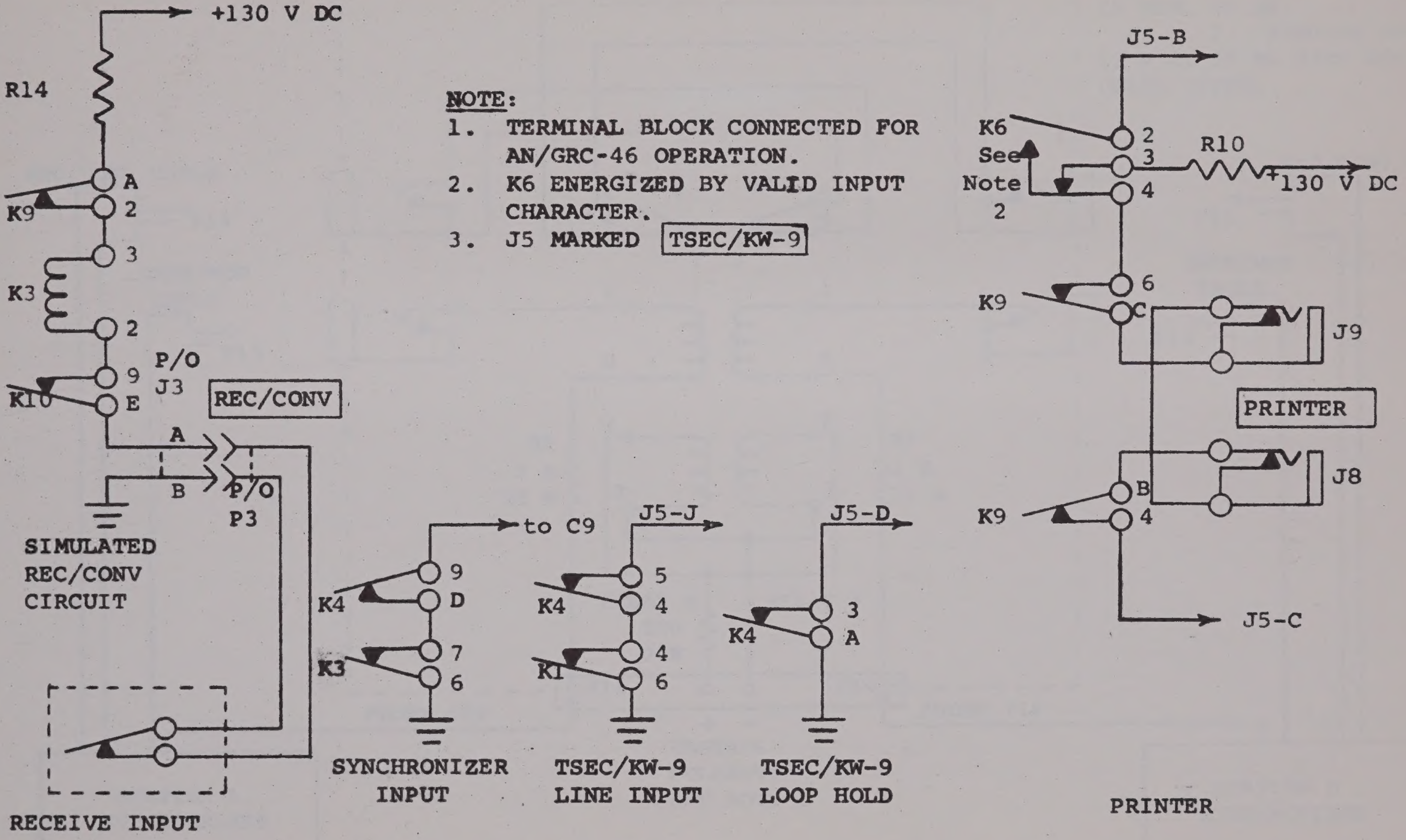
FIG. 25. SIMPLIFIED RELAY CIRCUIT, PLAIN RECEIVE.


P/O
J4
P/O
P4
+130 V DC
B
A
XMTR/MOD
SIMULATED
XMTR/MOD
CIRCUIT
K10
D
7
4
3
2
K5
SEE
NOTE
J5-H
K2
6
4
J5-A
K10
6
C
TO C9
K4
9
8
K10
2
A
J6
KBD AND TD
J7
B
4
J5-B
K6
2
4
K9
6
C
J9
PRINTER
J8
K9
B
4
J5-C
J5-D
K4
3
2
K1
4
6
J5-J
K4
5
B
TSEC/KW-9 LOOP
INPUT
TSEC/KW-9 LINE
HOLD
XMTR/MOD
SYNCHRONIZER
INPUT
HOME
COPY

NOTE:

1. TERMINAL BLOCK CONNECTED FOR AN/GRC-46 OPERATION.
2. K5 IS ENERGIZED WHEN A CHARACTER IS TO REACH THE XMTR/MOD.
3. J5 MARKED TSEC/KW-9

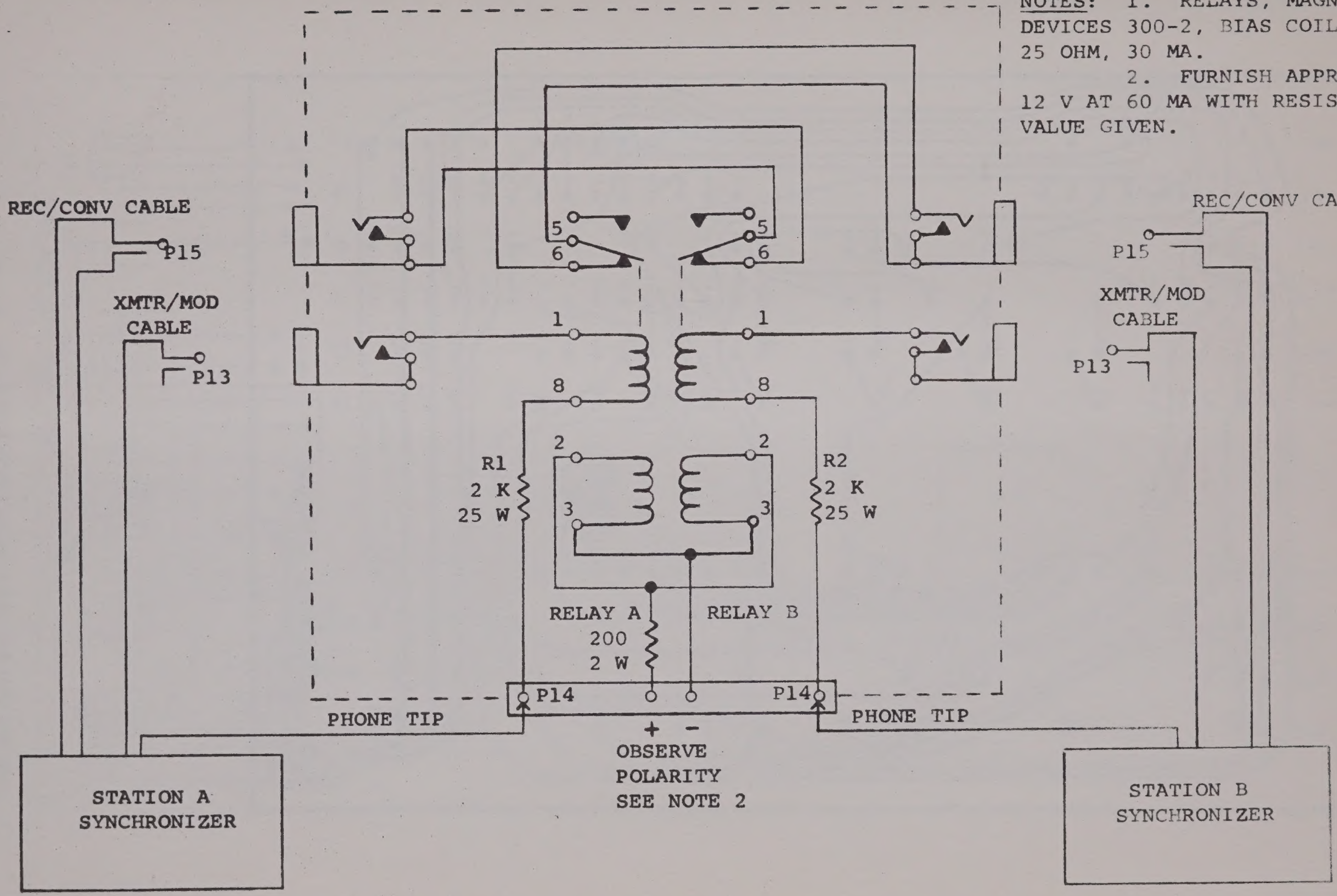
FIG. 26. SIMPLIFIED RELAY CIRCUIT, CIPHER SEND.


+130 V DC
R14
K9
A
2
3
K3
2
P/O
J3
9
K10
E
REC/CONV
A
B
P/O
P3
SIMULATED
REC/CONV
CIRCUIT
RECEIVE INPUT
to C9
K4
9
D
K3
7
6
SYNCHRONIZER
INPUT
J5-J
K4
5
4
K1
4
6
TSEC/KW-9
LINE INPUT
J5-D
K4
3
A
TSEC/KW-9
LOOP HOLD
J5-B
K6
See
Note
2
2
3
4
R10
+130 V DC
K9
6
C
J9
PRINTER
J8
K9
B
4
J5-C
PRINTER

NOTE:

1. TERMINAL BLOCK CONNECTED FOR AN/GRC-46 OPERATION.
2. K6 ENERGIZED BY VALID INPUT CHARACTER.
3. J5 MARKED TSEC/KW-9

FIG. 27. SIMPLIFIED RELAY CIRCUIT, CIPHER RECEIVE.


REC/CONV CABLE
P15
XMTR/MOD CABLE
P13
5
6
1
8
2
3
R1
2 K
25 W
RELAY A
200
2 W
RELAY B
R2
2 K
25 W
P14
P14
PHONE TIP
PHONE TIP
+ -
OBSERVE POLARITY SEE NOTE 2
STATION A SYNCHRONIZER
STATION B SYNCHRONIZER
REC/CONV CABLE
P15
XMTR/MOD CABLE
P13

NOTES: 1. RELAYS, MAGNETIC DEVICES 300-2, BIAS COIL 25 OHM, 30 MA.

2. FURNISH APPROX. 12 V AT 60 MA WITH RESISTOR VALUE GIVEN.

FIG. 28. BENCH TEST ASSEMBLY.

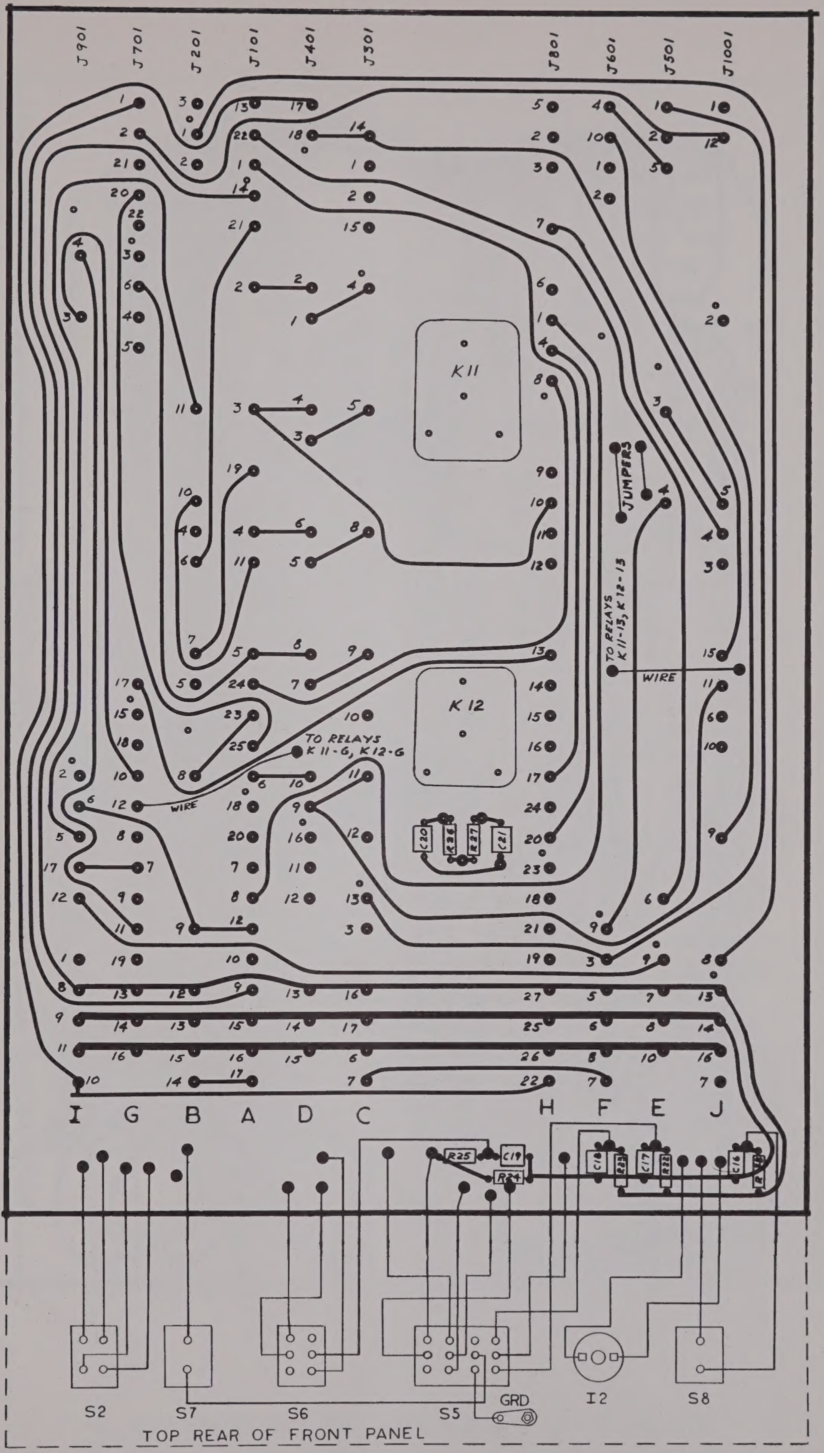

J901
J701
J201
J101
J401
J301
J801
J601
J501
J1001
K11
K12
JUMPERS
TO RELAYS K11-13, K12-13
WIRE
TO RELAYS K11-6, K12-6
WIRE
C20
R26
R27
C21
I
G
B
A
D
C
H
F
E
J
R25
C19
R24
C18
R23
C17
R22
C16
R21
S2
S7
S6
S5
GRD
I2
S8
TOP REAR OF FRONT PANEL

FIG. 29, INTERCONNECTING BOARD (TOP), WIRING DIAGRAM.

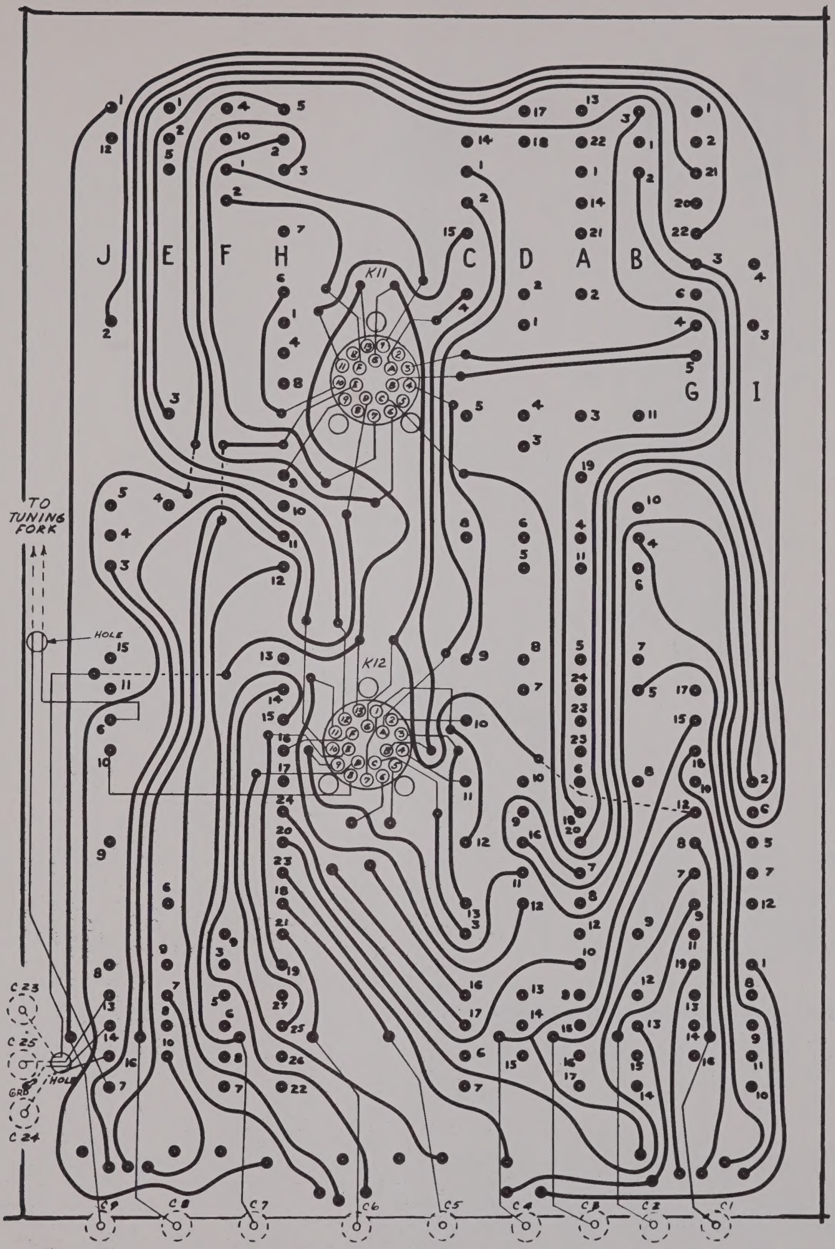

J
E
F
H
C
D
A
B
G
I
K11
K12
TO TUNING FORK
HOLE
C23
C25
GRD
HOLE
C24
C9
C8
C7
C6
C5
C4
C3
C2
C1

FIG. 30. INTERCONNECTING BOARD (BOTTOM), WIRING DIAGRAM.

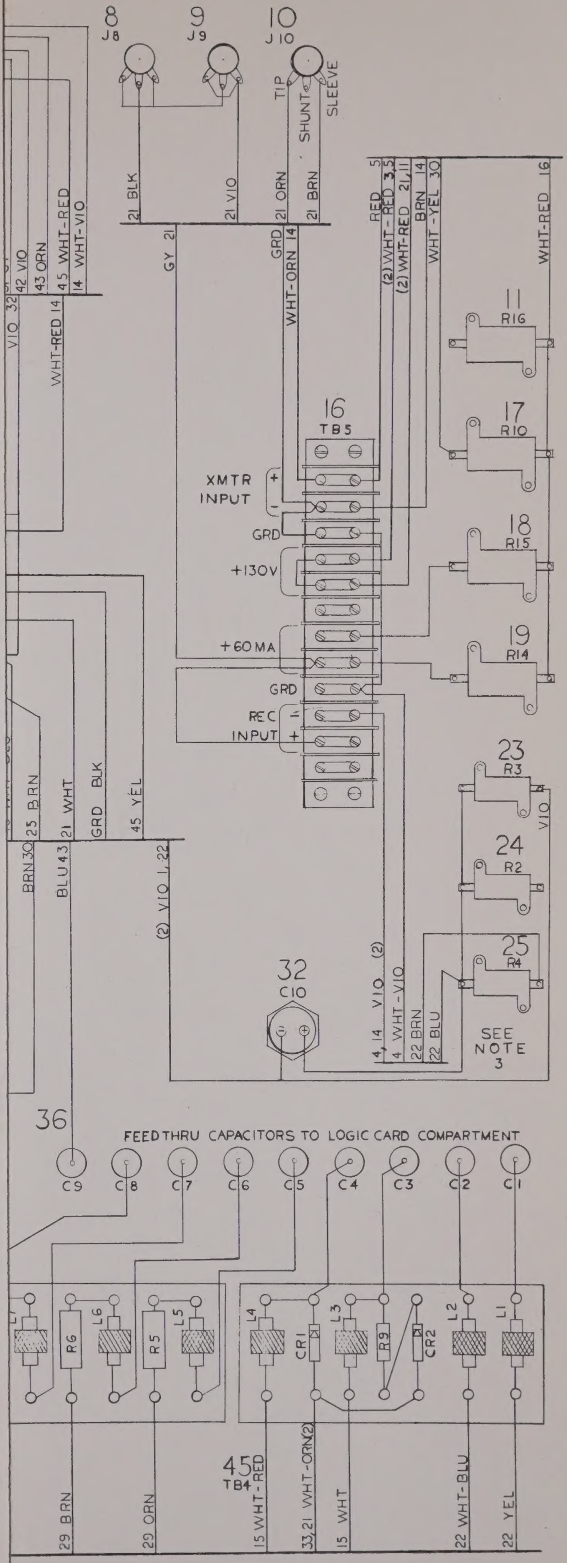
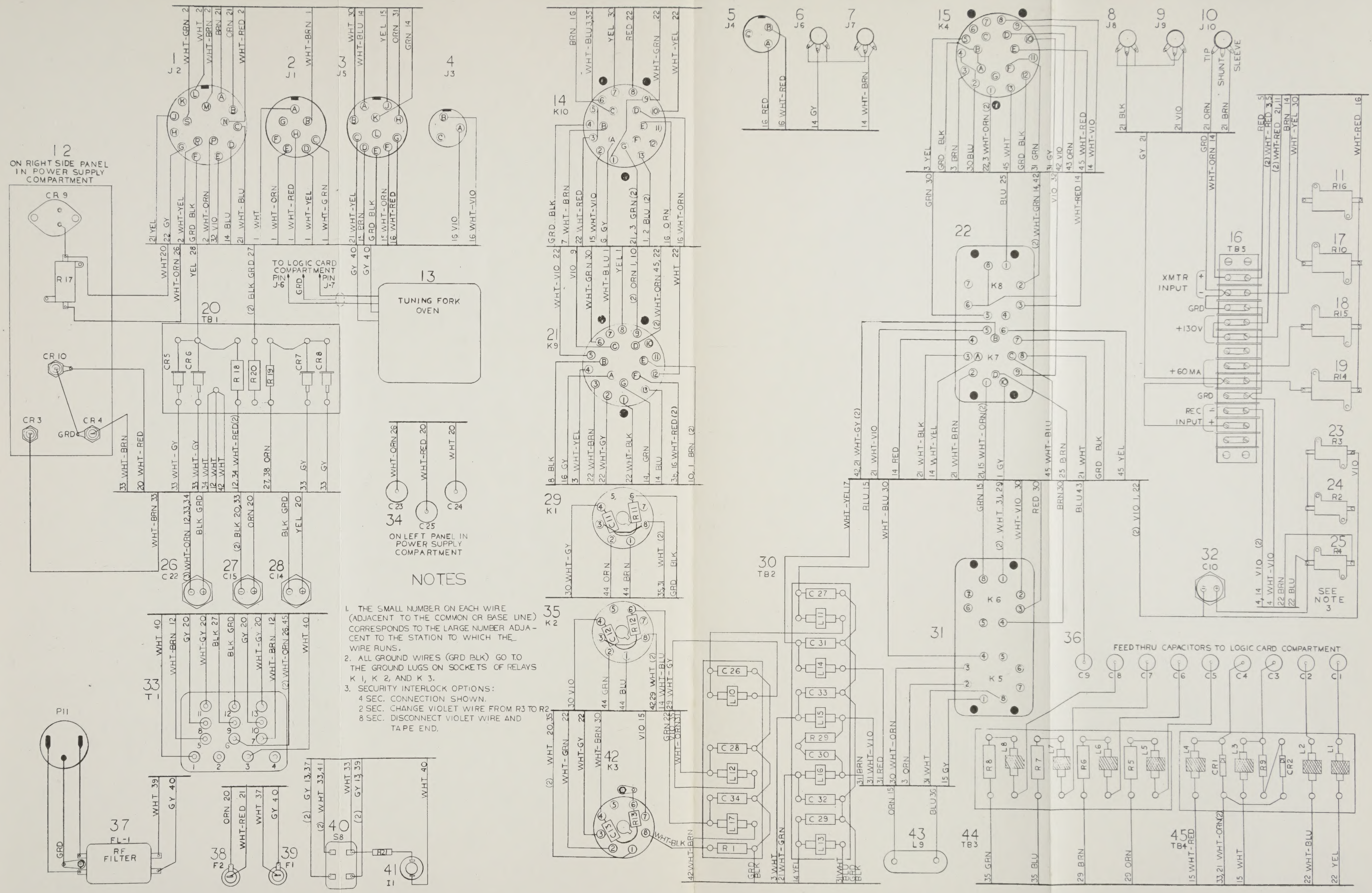

8
J8
9
J9
10
J10
TIP
SHUNT
SLEEVE
21 BLK
21 VIO
21 ORN
21 BRN
RED 5
(2) WHT-RED 3,5
(2) WHT-RED 21,11
BRN 14
WHT-YEL 30
WHT-RED 16
GY 21
GRD
WHT-ORN 14
VIO 32
42 VIO
43 ORN
45 WHT-RED
14 WHT-VIO
WHT-RED 14
11
R16
17
R10
16
TB5
XMTR
INPUT
+
−
GRD
+130V
+60 MA
GRD
REC
INPUT
−
+
18
R15
19
R14
23
R3
VIO
24
R2
25
R4
SEE
NOTE
3
25 BRN
21 WHT
GRD BLK
45 YEL
BRN 30
BLU 43
(2) VIO 1, 22
32
C10
4, 14 VIO (2)
4 WHT-VIO
22 BRN
22 BLU
36
FEED THRU CAPACITORS TO LOGIC CARD COMPARTMENT
C9
C8
C7
C6
C5
C4
C3
C2
C1
L7
R6
L6
R5
L5
L4
CR1
L3
R9
CR2
L2
L1
45
TB4
29 BRN
29 ORN
15 WHT-RED
33,21 WHT-ORN(2)
15 WHT
22 WHT-BLU
22 YEL

FIG. 31. MAIN CHASSIS, WIRING DIAGRAM


1
J2
2
J1
3
J5
4
J3
12
ON RIGHT SIDE PANEL IN POWER SUPPLY COMPARTMENT
CR 9
R 17
CR 10
CR 3
CR 4
GRD
TO LOGIC CARD COMPARTMENT
PIN J-6
GRD
PIN J-7
13
TUNING FORK OVEN
20
TB1
CR5
CR6
R 18
R 20
R 19
CR7
CR8
26
C 22
27
C15
28
C14
34
C23
C25
C24
ON LEFT PANEL IN POWER SUPPLY COMPARTMENT
33
T1
P11
37
FL-1
RF FILTER
38
F2
39
F1
40
S8
R21
41
I1
14
K10
21
K9
29
K1
35
K2
42
K3
5
J4
6
J6
7
J7
15
K4
8
J8
9
J9
10
J10
TIP
SHUNT
SLEEVE
22
K8
K7
K6
31
K5
16
TB5
XMTR INPUT
GRD
+130V
+60 MA
GRD
REC INPUT
11
R16
17
R10
18
R15
19
R14
23
R3
24
R2
25
R4
SEE NOTE 3
32
C10
30
TB2
36
FEED THRU CAPACITORS TO LOGIC CARD COMPARTMENT
C9
C8
C7
C6
C5
C4
C3
C2
C1
43
L9
44
TB3
45
TB4

NOTES

1. THE SMALL NUMBER ON EACH WIRE (ADJACENT TO THE COMMON OR BASE LINE) CORRESPONDS TO THE LARGE NUMBER ADJACENT TO THE STATION TO WHICH THE WIRE RUNS.
2. ALL GROUND WIRES (GRD BLK) GO TO THE GROUND LUGS ON SOCKETS OF RELAYS K 1, K 2, AND K 3.
3. SECURITY INTERLOCK OPTIONS:
   - 4 SEC. CONNECTION SHOWN.
   - 2 SEC. CHANGE VIOLET WIRE FROM R3 TO R2
   - 8 SEC. DISCONNECT VIOLET WIRE AND TAPE END.

FIG. 31. MAIN CHASSIS, WIRING DIAGRAM

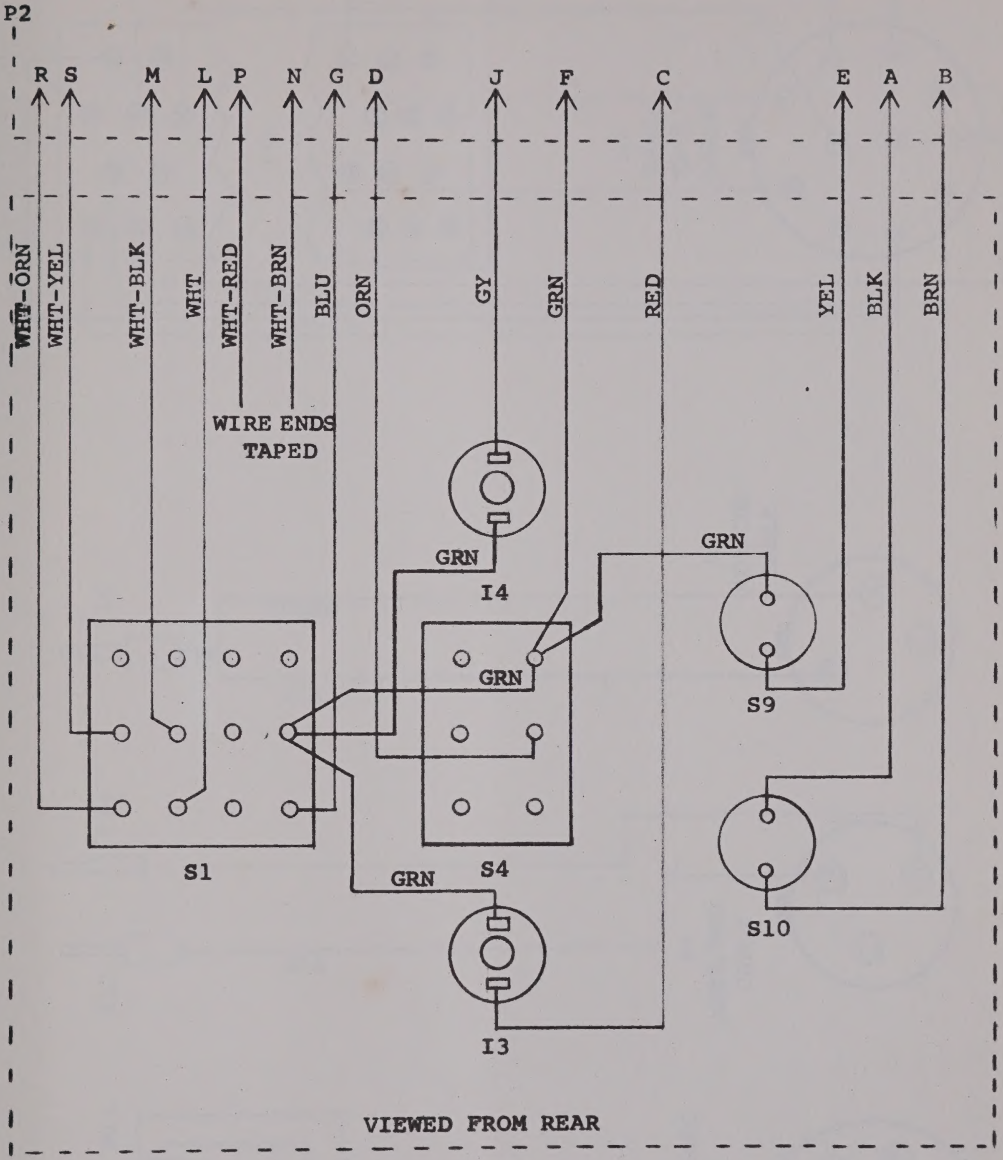

P2
R
S
M
L
P
N
G
D
J
F
C
E
A
B
WHT-ORN
WHT-YEL
WHT-BLK
WHT
WHT-RED
WHT-BRN
BLU
ORN
GY
GRN
RED
YEL
BLK
BRN
WIRE ENDS TAPED
GRN
I4
GRN
GRN
S9
S1
S4
GRN
S10
I3
VIEWED FROM REAR

FIG. 32. REMOTE CONTROL BOX, WIRING DIAGRAM.

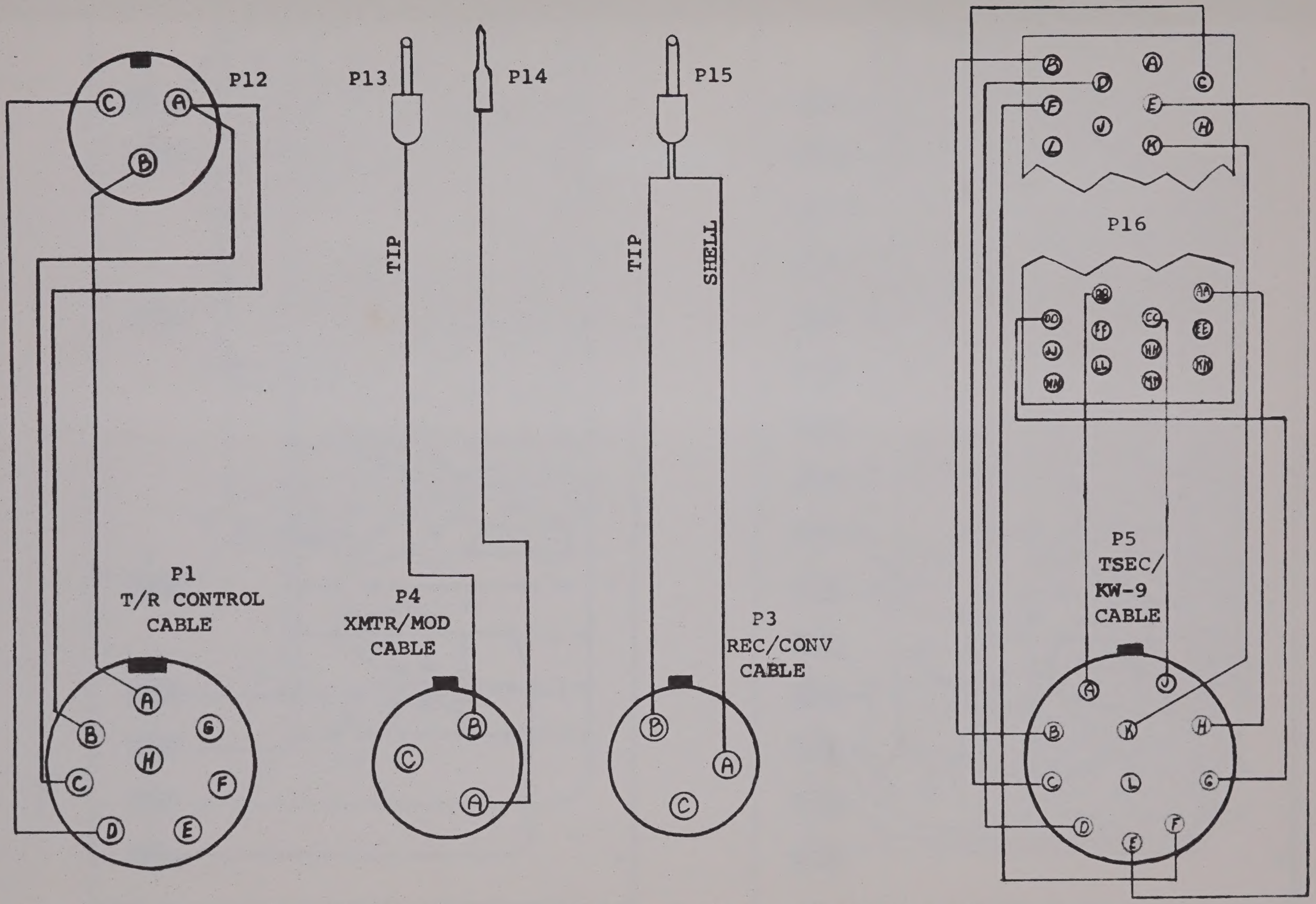

P12
P13
P14
P15
TIP
TIP
SHELL
P16
P1
T/R CONTROL
CABLE
P4
XMTR/MOD
CABLE
P3
REC/CONV
CABLE
P5
TSEC/
KW-9
CABLE
A
B
C
D
E
F
G
H
J
K
L
AA
BB
CC
DD
EE
FF
HH
JJ
KK
LL
MM
NN

FIG. 33. CABLE CONNECTORS, WIRING DIAGRAM.

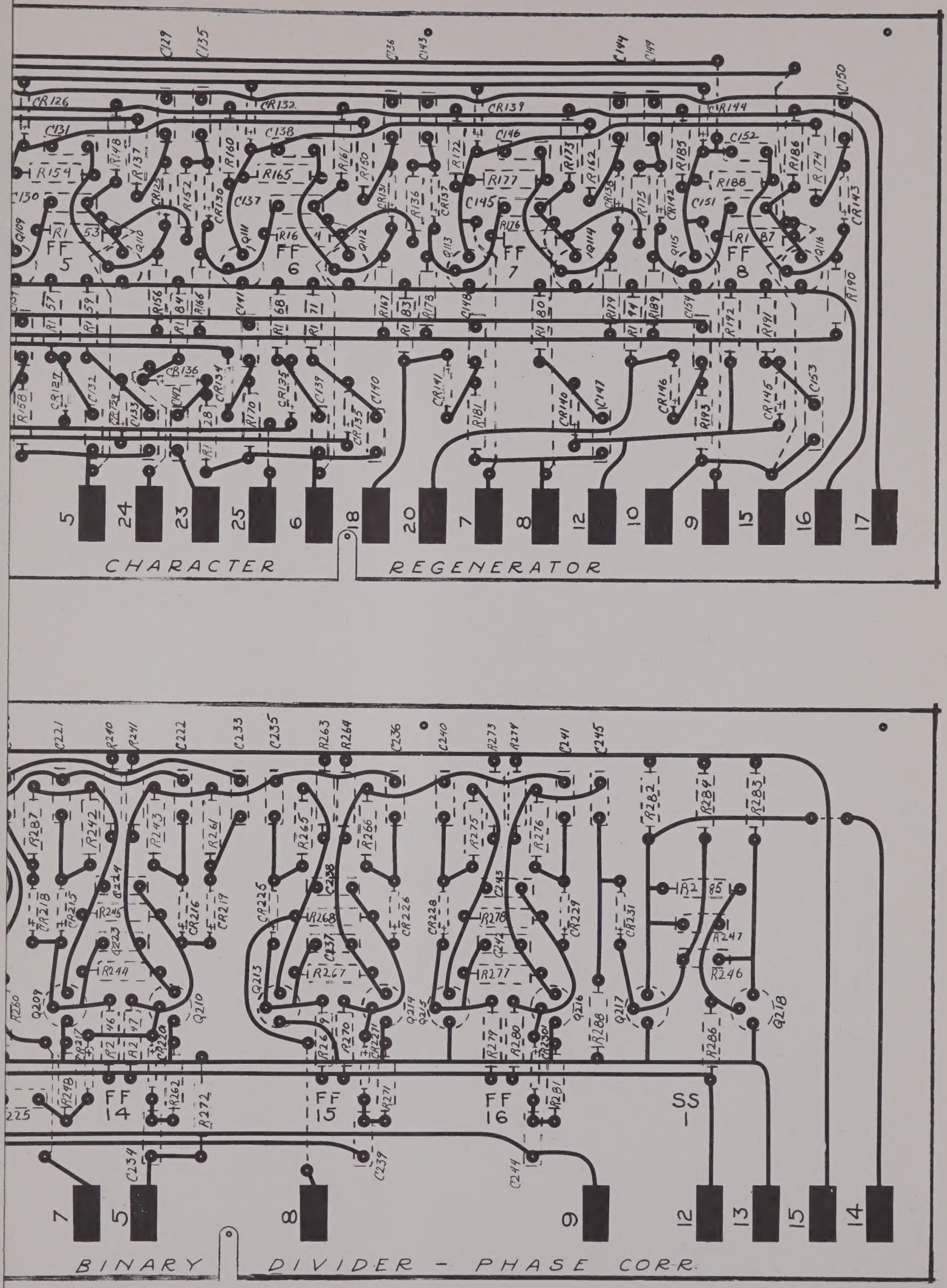

CHARACTER REGENERATOR
FF 5
FF 6
FF 7
FF 8
5
24
23
25
6
18
20
7
8
12
10
9
15
16
17
BINARY DIVIDER - PHASE CORR
FF 14
FF 15
FF 16
SS 1
7
5
8
9
12
13
15
14

FIG. 34. CARD A AND CARD B, WIRING DIAGRAM.

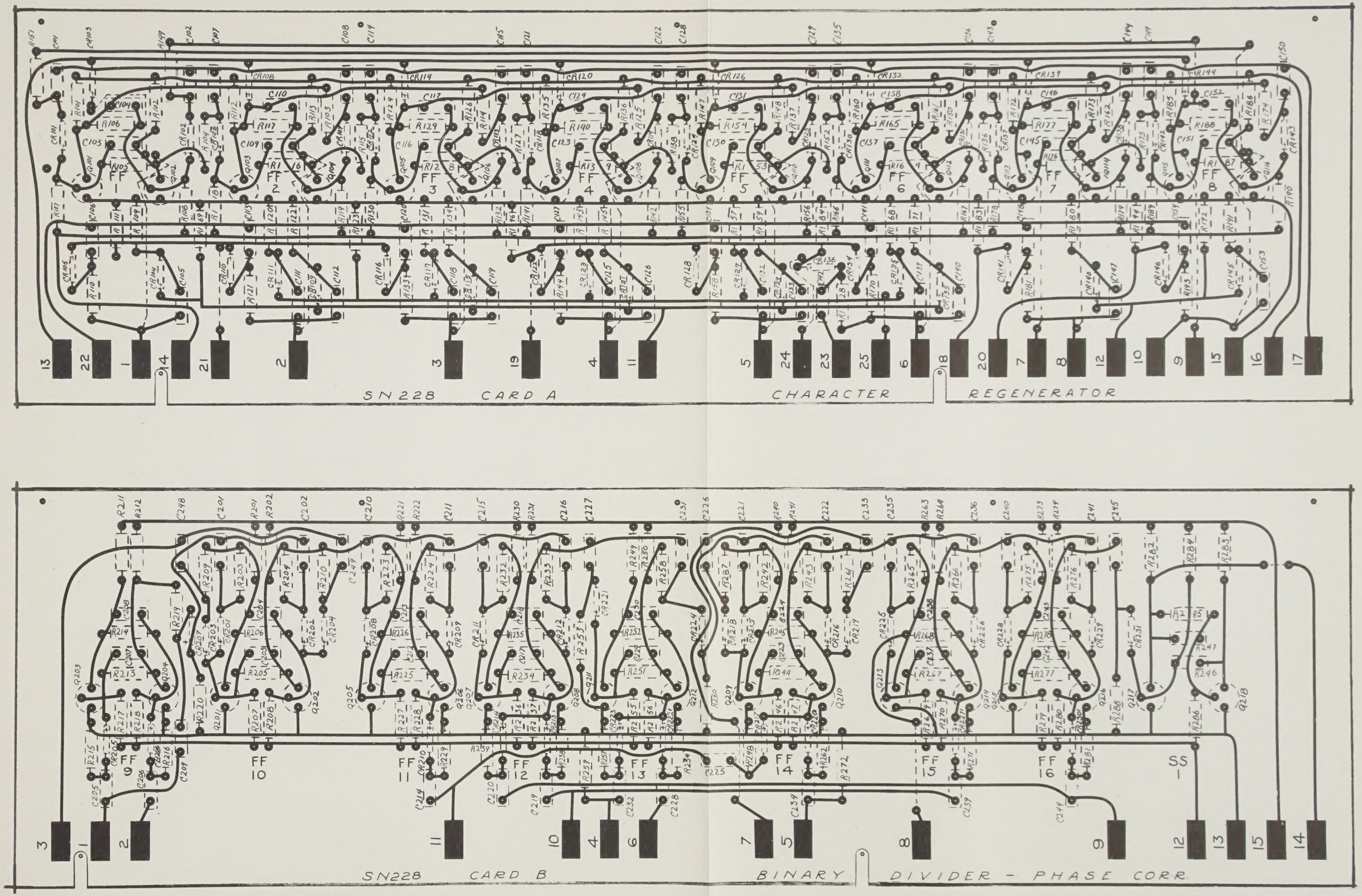

SN228 CARD A CHARACTER REGENERATOR
13
22
1
14
21
2
3
19
4
11
5
24
23
25
6
18
20
7
8
12
10
9
15
16
17
FF 1
FF 2
FF 3
FF 4
FF 5
FF 6
FF 7
FF 8
SN228 CARD B BINARY DIVIDER - PHASE CORR.
3
1
2
11
10
4
6
7
5
8
9
12
13
15
14
FF 9
FF 10
FF 11
FF 12
FF 13
FF 14
FF 15
FF 16
SS 1

FIG. 34. CARD A AND CARD B, WIRING DIAGRAM.

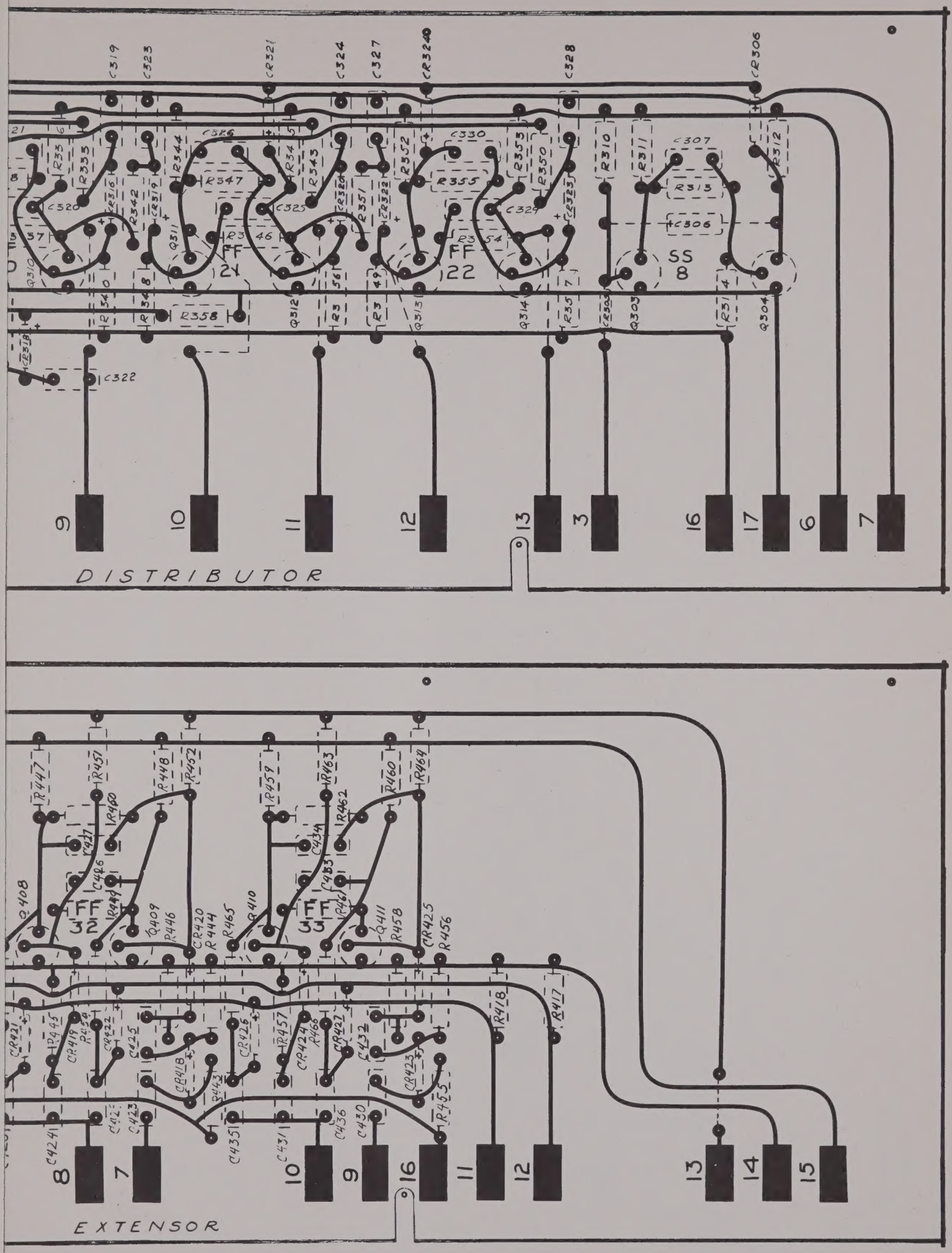

C319
C323
CR321
C324
C327
CR324
C328
CR306
C326
R344
R347
R333
C320
R342
CR319
Q311
FF
21
R358
C322
Q310
CR318
C325
R345
R343
CR320
R351
CR322
R352
C330
R355
R353
R350
CR323
FF
22
C329
Q312
Q313
Q314
R310
R311
C307
R313
R312
C306
SS
8
Q303
Q304
9
10
11
12
13
3
16
17
6
7
DISTRIBUTOR
R447
R451
R448
R452
R459
R463
R460
R464
R450
R462
C427
C426
C434
C433
FF
32
FF
33
Q408
Q409
Q410
Q411
R446
CR420
R444
R465
R458
CR425
R456
R418
R417
CR421
R445
CR419
R454
CR422
C425
CR418
R443
CR426
R457
CR424
R466
CR427
C432
CR423
R455
C424
C423
C435
C431
C436
C430
8
7
10
9
16
11
12
13
14
15
EXTENSOR

FIG. 35. CARD C AND CARD D, WIRING DIAGRAM.

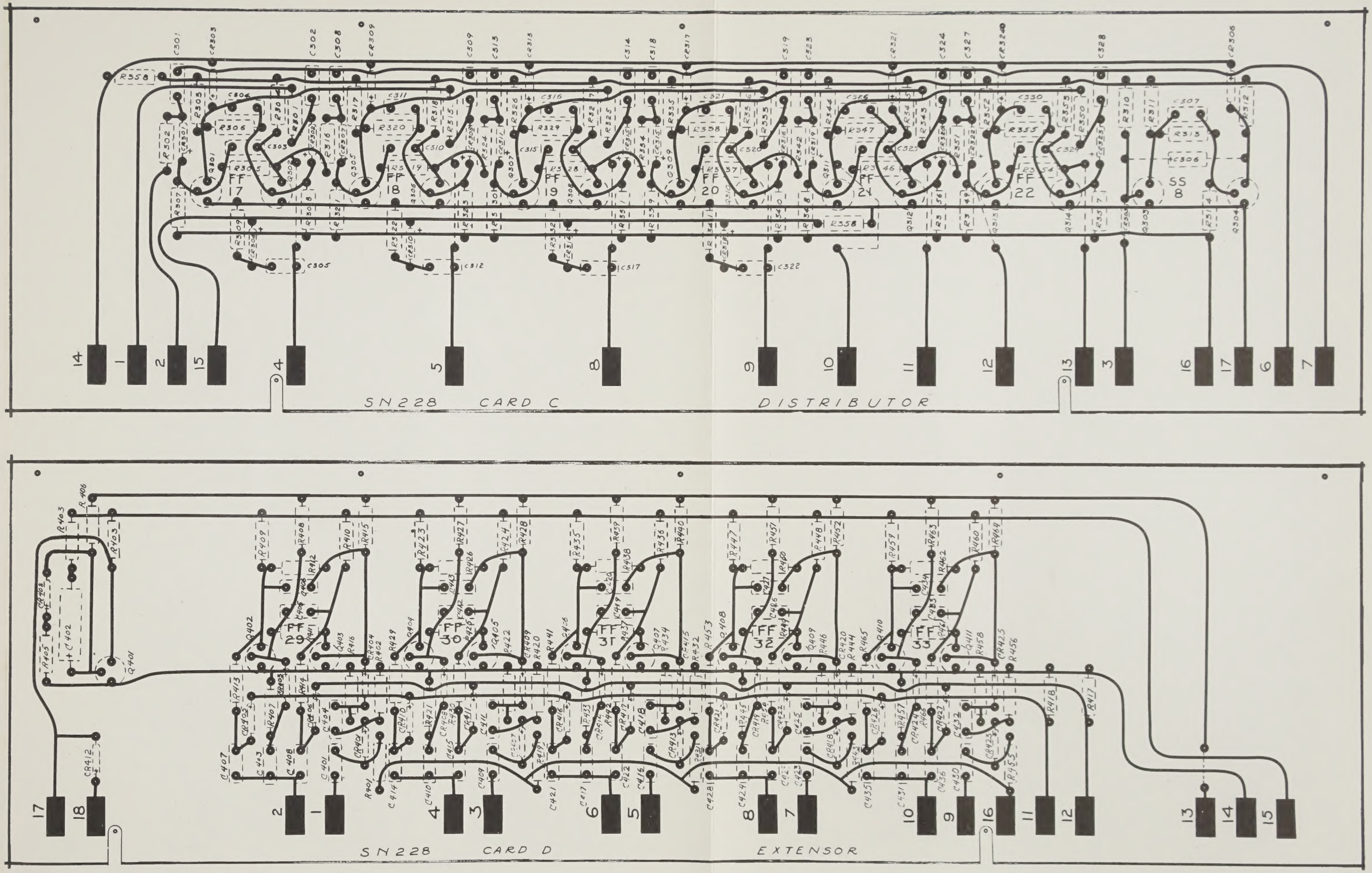

SN228 CARD C DISTRIBUTOR
FF 17
FF 18
FF 19
FF 20
FF 21
FF 22
SS 8
14
1
2
15
4
5
8
9
10
11
12
13
3
16
17
6
7
SN228 CARD D EXTENSOR
FF 29
FF 30
FF 31
FF 32
FF 33
17
18
2
1
4
3
6
5
8
7
10
9
16
11
12
13
14
15

FIG. 35. CARD C AND CARD D, WIRING DIAGRAM.

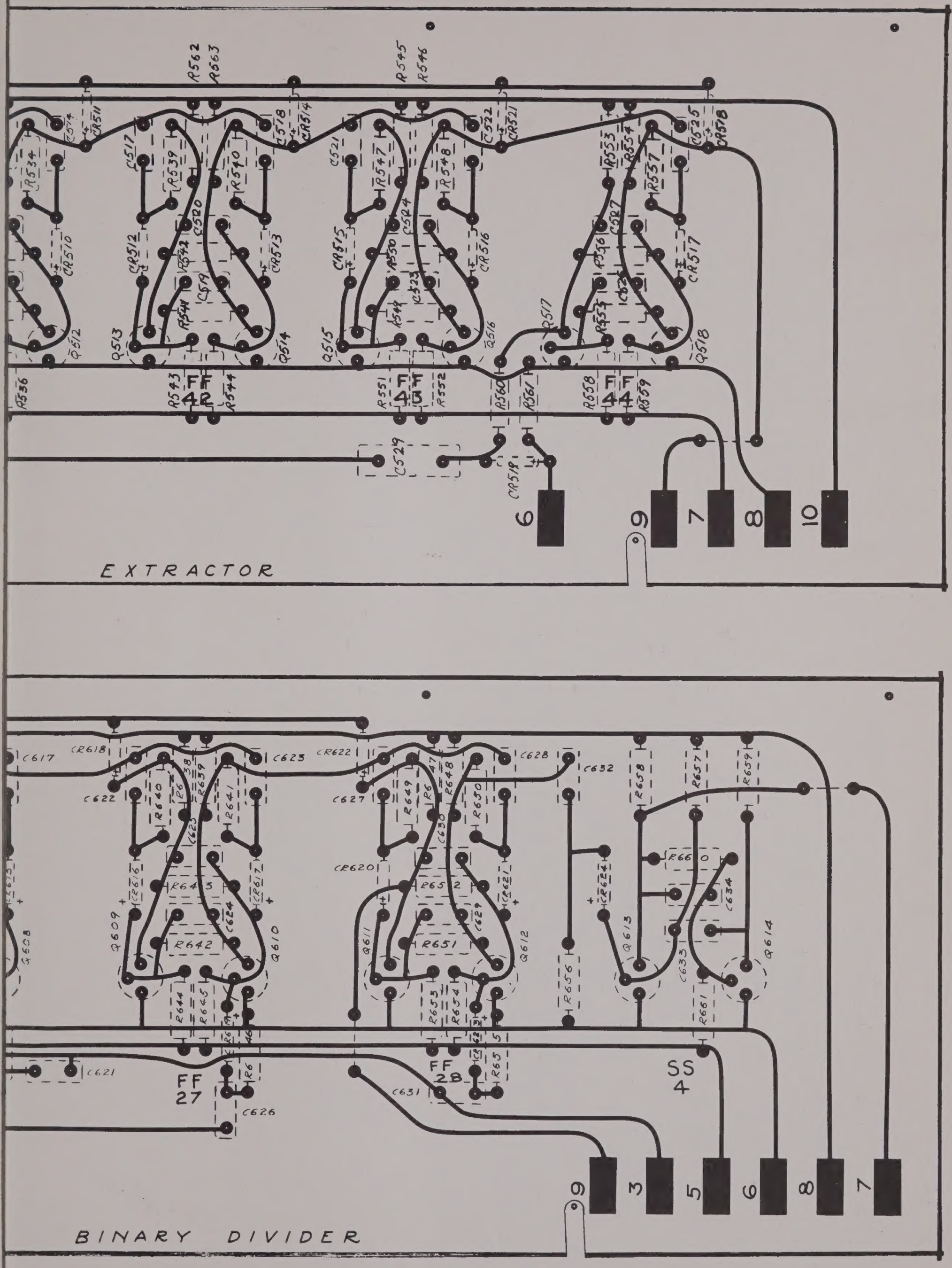

R562
R563
R545
R546
CR511
CR514
CR521
CR518
C517
C518
C521
C522
C525
R534
R539
R540
R547
R548
R553
R554
R557
CR510
CR512
CR513
CR515
CR516
CR517
C520
C524
C527
R542
R550
R556
C519
C523
C526
R541
R549
R555
Q512
Q513
Q514
Q515
Q516
Q517
Q518
R536
R543
R544
R551
R552
R558
R559
R560
R561
FF 42
FF 43
FF 44
C529
CR519
6
9
7
8
10
EXTRACTOR
C617
CR618
C622
C623
CR622
C627
C628
C632
R640
R638
R639
R641
R649
R647
R648
R650
R658
R657
R659
CR616
CR617
CR620
CR621
CR624
R643
R652
R660
C625
C630
C634
R642
R651
C624
C629
C633
CR615
Q608
Q609
Q610
Q611
Q612
Q613
Q614
R644
R645
R646
R653
R654
R655
R656
R661
C621
C626
C631
FF 27
FF 28
SS 4
9
3
5
6
8
7
BINARY DIVIDER

FIG. 36. CARD E AND CARD F, WIRING DIAGRAM.

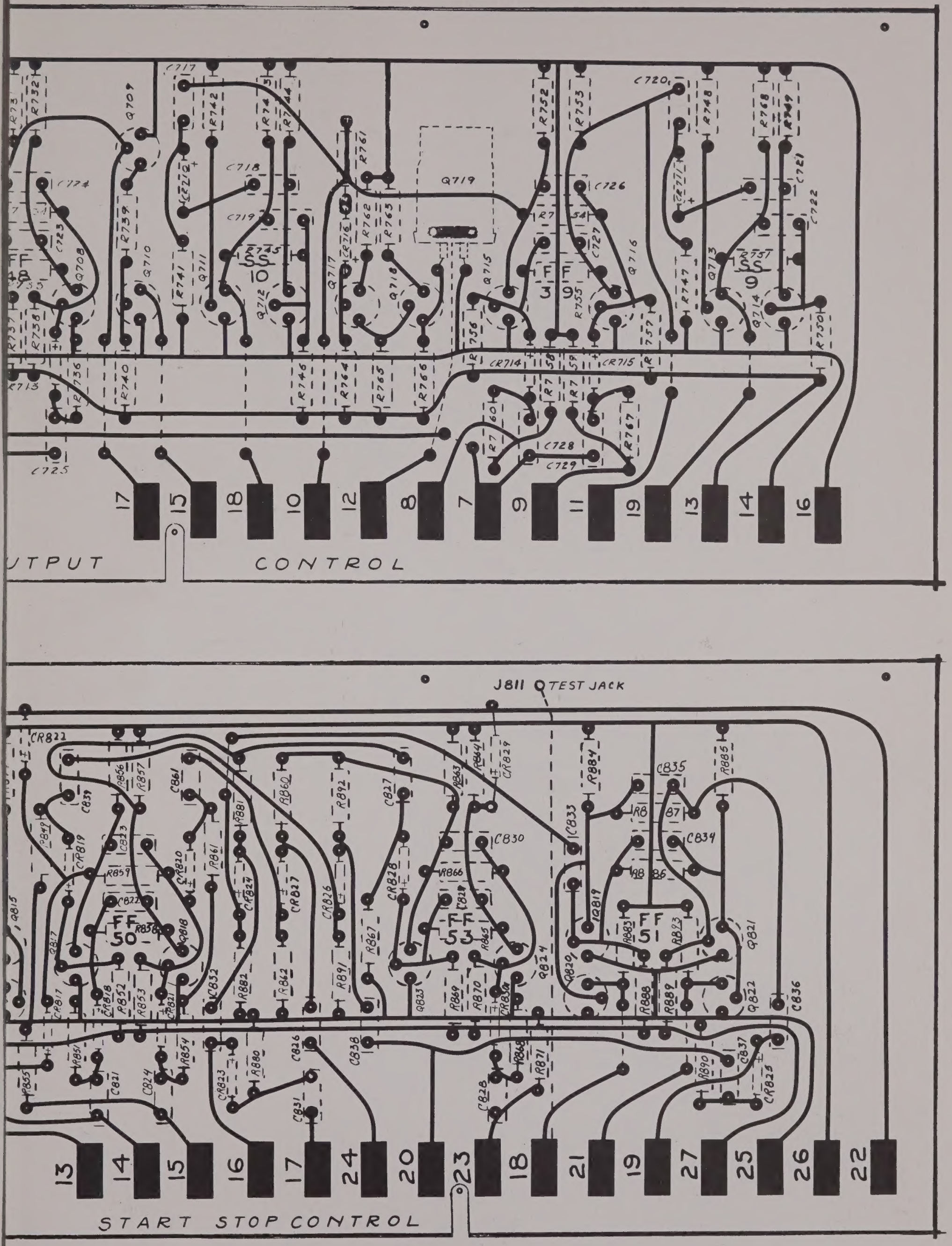

Q719
FF 39
SS 10
SS 9
17 15 18 10 12 8 7 9 11 19 13 14 16
UTPUT CONTROL
J811 TEST JACK
FF 50
FF 53
FF 51
13 14 15 16 17 24 20 23 18 21 19 27 25 26 22
START STOP CONTROL

FIG. 37. CARD G AND CARD H, WIRING DIAGRAM.

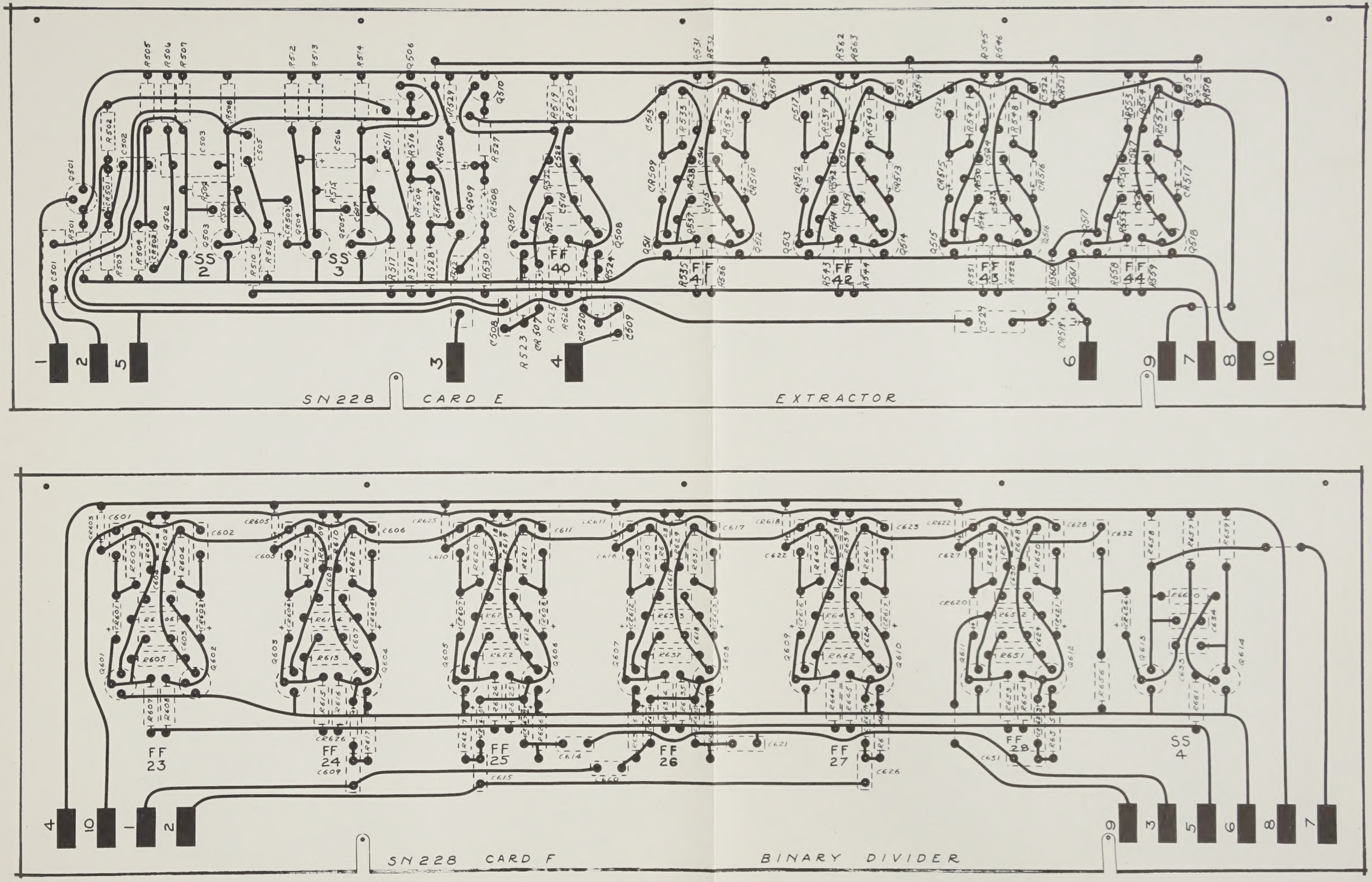
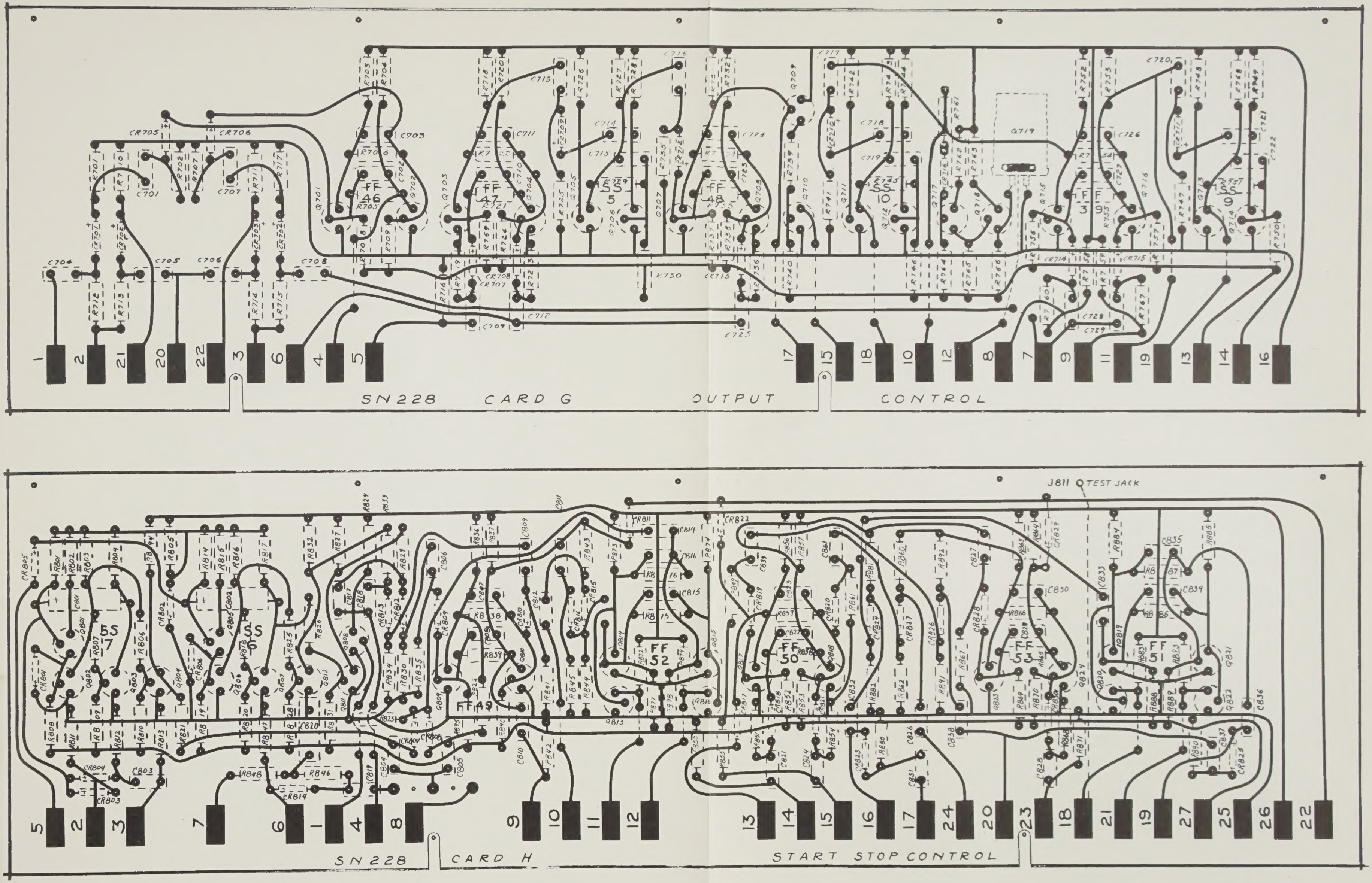

SN228 CARD E
EXTRACTOR
SS 2
SS 3
FF 40
FF 41
FF 42
FF 43
FF 44
1
2
5
3
4
6
9
7
8
10
SN228 CARD F
BINARY DIVIDER
FF 23
FF 24
FF 25
FF 26
FF 27
FF 28
SS 4
4
10
1
2
9
3
5
6
8
7

FIG. 36. CARD E AND CARD F, WIRING DIAGRAM.



SN228 CARD G OUTPUT CONTROL
FF 46
FF 47
SS 5
FF 48
SS 10
Q719
FF 39
SS 9
SN228 CARD H START STOP CONTROL
J811 TEST JACK
SS 7
SS 6
FF 49
FF 52
FF 50
FF 53
FF 51

FIG. 37. CARD G AND CARD H, WIRING DIAGRAM.